STIC Search Report
EIC 2800

STIC Database Tracking Number: 116164

TO:	From:
Monica Lewis **Location:** **Art Unit : 2822** **Monday, March 08, 2004** **Case Serial Number: 09/829797**	**Bode Fagbohunka** **Location: EIC 2800** **Jeff 4A58** **Phone: 571-272-2541** **bode.fagbohunka@uspto.gov**

Search Notes

Examiner **Monica Lewis**

Please find attached the results of your search for **09/829797**. The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

Bode Fagbohunka

116164

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 3/5/04 Serial # 09/899,797 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2892 Phone 272-1835 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 03-05-04 P03:59 IN

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ___ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-7

Problem See Page 2 lines 25-33

Solution: " " 3 " 1-8

Staff Use Only	Type of Search	Vendors
Searcher: Sode Tassunda	Structure (#)	STN
Searcher Phone: 272-2541	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit ✓
Date Searcher Picked Up: 03-08-04	Fulltext	Lexis-Nexis
Date Completed: 03-08-04	Patent Family ✓	WWW/Internet
Searcher Prep/Rev Time: 40	Other	Other
Online Time: 240		

Amendments to the Claims

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above a layered structure that increases structural integrity of the bond pad structure, wherein the layered structure comprises a top and bottom metal layer, a plurality of intermediate metal layers, at least one layer of dielectric material, and a plurality of equally spaced parallel via lines that connect the top and bottom metal layers and partition the at least one dielectric area to form isolated areas filled with dielectric material, and wherein each intermediate metal layer is divided into a plurality of separated segments that form t-shaped cross-sections with the via lines.

2. (Original) A semiconductor device as claimed in claim 1, wherein the via lines are lines of tungsten.

3. (Previously Amended) A semiconductor device as claimed in claim 1, wherein a stack of layered structures is present.

4. (Original) A semiconductor device as claimed in claim 3, wherein the metal layer in each layered structure is a metal plate.

5. (Original) A semiconductor device as claimed in claim 4, wherein the top and bottom metal layers of the stack are metal plates, and the intermediate metal layer or layers are parallel metal lines.

6. (Original) A semiconductor device as claimed in claim 5, wherein the metal lines are patterned in the form of a grid.

7. (Previously Amended) A semiconductor device as claimed in claim 1, wherein the via lines are patterned in the form of a grid.

8-11 (Cancelled)

ABSTRACT:

The invention relates to a semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, but preferably a stack of layered structures, wherein the layered structure comprises a metal layer and a layer of a dielectric material. In the layer of dielectric material via lines are present and arranged in such a way that the metal layers and the via lines form isolated areas filled with the dielectric material.

Fig. 3

Semiconductor device

The present invention relates to the field of semiconductor devices and more specifically to integrated circuits (ICs) having bond pads incorporated therein. More particularly, the invention relates to a semiconductor device comprising a new bond pad structure wherein cracking is eliminated, or at least reduced. More in detail, the present invention relates to a semiconductor device comprising a bond pad structure, which enables wire bonding and probing to be carried out without the induction of - or at least with a reduced occurrence of - cracks in the intermetal dielectrics applied.

In state-of-the-art IC technology, bond pads consist of a multilayer aluminum metallization, generally with one or more layers of e.g. titanium or titanium nitride. Bond pads are present for attaching solder, wire or other bonding elements, especially constructed from aluminum, gold or copper.

Bond pads are typically disposed above one or more layers or stacks of brittle and/or soft intermetal dielectric materials, such as silicon oxides and organic materials.

Bond pad cracks can occur during ultrasonic wire bonding or even through probing. Cracks can lead to reliability problems, especially when low-k spin-on dielectrics, such as hydrogen silsesquioxane (HSQ), are used. Such dielectrics, and especially HSQ, are more brittle than other oxides, such as tetraethoxysilane-based oxides. In HSQ layers cracks can therefore more easily propagate than in other oxides. Similar problems occur with aerogels, organic polyimides, parylenes and the like, which all have low dielectric constants as compared to silicon oxides, but are structurally and mechanically weaker than these oxides.

In the art, there is a need for structures or methods to prevent or at least reduce the occurrence of bond pad cracking.

It has been proposed in EP-A-0 875 934 to dispose a patterned reinforcing structure in a dielectric layer disposed under the bond pad. The basic principle laid down in this document is that through the use of metal grids mechanical reinforcement of the dielectric stack can be achieved and damage due to bonding can be prevented. More in detail, this known reinforced structure is manufactured by forming a metal layer, patterning the metal layer in a predetermined area in accordance with a predetermined pattern having a

plurality of vacant areas, forming a dielectric layer above the patterned metal layer, and filling the vacant areas in the patterned metal layer. Finally, a bond pad is formed on the dielectric layer above the patterned metal layer.

The known reinforcing structure may be a joined or interconnected grid or a crosshatch structure with a plurality of voids or vacant areas for containing and accommodating a large portion of weak dielectric material such as the said HSQ and the like. The grid structure is planar with a thickness below the thickness of the intermetal dielectric stack. In another embodiment, the reinforcing structure includes a repeating and non-interconnected pattern such as a crucifix pattern arranged in a regular manner. Other structures such as spirals have been described as well.

The present inventors have intensively studied two of the structures known from EP-A-0 875 934:

- the crosshatch structure, wherein at each metal level, under the bond pad, a crosshatch grid of metal was inserted to confine mechanically relatively weak HSQ into square reservoirs created by the grid; and
- the crucifix structure. This structure provides a more open metal pattern as compared with the crosshatch structure, allowing HSQ to flow more easily into the voids.

In the crosshatch structure, the metal line widths and spacings were designed to confine much of the HSQ into the reservoirs while minimizing the area of each reservoir, so that the HSQ layer is spared the direct mechanical impact of bonding. Vias were formed only at the pad periphery.

In the crucifix structure, the more open pattern allows the HSQ to flow more easily in the voids present in the structure. By virtue thereof, the amount of HSQ remaining over the metal lines is reduced slightly further as compared to the crosshatch structure.

Both known structures have, however, a continuous TEOS dielectric layer between the metal layers, which dielectric layer can be cracked due to bonding or probing.

The present invention aims to solve or at least reduce this problem.

In accordance with the present invention, it has now been found that elimination, or at least reduction of bond pad cracking can be achieved by isolating the intermetal dielectrics with metal lines and via lines. Further, the bond pad structure of the semiconductor device according to the present invention prevents the propagation of any cracks that are formed. Moreover, metal peel off during bonding is diminished. Metal peel off is a failure mode occurring at the interface between a top metal plate and intermetal dielectrics.

More in detail, the present invention is based on the principle that use is made of via lines together with metal lines to completely isolate intermetal dielectrics. For this purpose, the invention relates to a semiconductor device comprising a bond pad structure, which bond pad structure comprises a bond pad disposed above at least one layered structure, but preferably a stack of layered structures, wherein the layered structure comprises a metal layer and a layer of a dielectric material, characterized in that via lines are present in the layer of dielectric material, which via lines are arranged in such a way that the metal layers and the via lines form isolated areas filled with the dielectric material.

Furthermore, the present invention relates to a method of manufacturing a semiconductor device as described above, which method comprises the steps of:

(a) forming a metal layer;

(b) forming a dielectric layer;

(c) patterning via lines or via grids in the dielectric layer;

(d) filling the patterned via lines or via grids with a conductive material, such as a metal, and preferably tungsten or copper; and

(e) applying a metal bond pad on top of the dielectric layer and the filled via lines or via grids.

By the use of via lines connected to the metal layer, the adhesion between the top metal plate and the underlying layers is enhanced, so that metal peal off occurs no longer or less often.

Without being bound by a very specific theory, it is assumed that when a crack is formed in an intermetal dielectric, the system releases elastic energy and gains surface energy. Based on thermodynamic principles, the crack should not form when the amount of elastic energy to be released is smaller than the amount of surface energy to be gained. Since elastic energy is proportional to the volume of the dielectric and surface energy is proportional to the surface area of the dielectric, the present invention makes use of a small volume-to-area ratio by using small feature sizes. Therefore, the via lines, or optionally the via grids, are advantageously arranged in such a way that the volume-to-surface area is - dependent on the dielectric material used - adjusted such that the amount of elastic energy to be released when a crack is formed is smaller than the amount of surface energy to be gained when said crack is formed.

Apart from the above, it is noted that in the art vias are normally patterned in square or round pillars. Multiple rows of such pillars, shifted with respect to each other, are in use in e.g. seal rings to prevent the propagation of cracks. However, in accordance with the

present invention, via lines, e.g. in the form of a via grid, avoid the formation of cracks as well as the propagation in case a crack is formed anyway. Moreover, bonding stress can be released by ductile properties of the via-metal, in particular when tungsten is used as the via-metal.

The present invention will be described in further detail with reference to the drawings, wherein

Fig. 1 is a schematic top view of the bond pad structure of the semiconductor device according to the invention;

Figs. 2 and 3 are cross-sections of two embodiments of the bond pad structure of the semiconductor device of the present invention, wherein the upper cross-sections of Figs. 2 and 3 are cross-sections of the structure of Fig. 1 indicated by means of the upper arrow, while the lower cross-sections of Figs. 2 and 3 are cross-sections of the structure of Fig. 1 indicated by means of the lower arrow.

Fig. 1 shows a schematic top view of the bond pad structure of the semiconductor device of the present invention at via level. This top view shows the crosshatch feature of the structures. Intermetal dielectrics are isolated by metal and via lines. The details will become clear from Figs. 2 and 3.

In Fig. 2, an embodiment is shown wherein each layered structure comprises a metal plate 1. Intermetal dielectrics 4 are isolated by two adjacent metal plates 1 and, in the vertical direction, by via lines or via grids 3.

Fig. 3 shows the embodiment wherein the top and bottom layered structures comprise a metal plate 1, while the intermediate layered structures are formed by metal lines or metal grids 2. Intermetal dielectrics 4 are isolated by the top and bottom metal plates 1 and by the metal lines or metal grids 2 and via lines or via grids 3 in between.

The distances between the via lines or via grids in a particular layer structure are chosen to be such that the volume-to-surface area ratio of the dielectrics 4 in the direction parallel to the bond pad is sufficiently small to prevent crack formation during probing or bonding. For example, when the dielectrics thickness is 1 μm, the width and length of the dielectric block should be smaller than 10 μm. Normally, a bond pad size is about 80 x 80 μm. Without the isolation of the dielectric layers cracks can easily form.

On top of the structures in accordance with the invention a bond pad, preferably of Al, is applied.

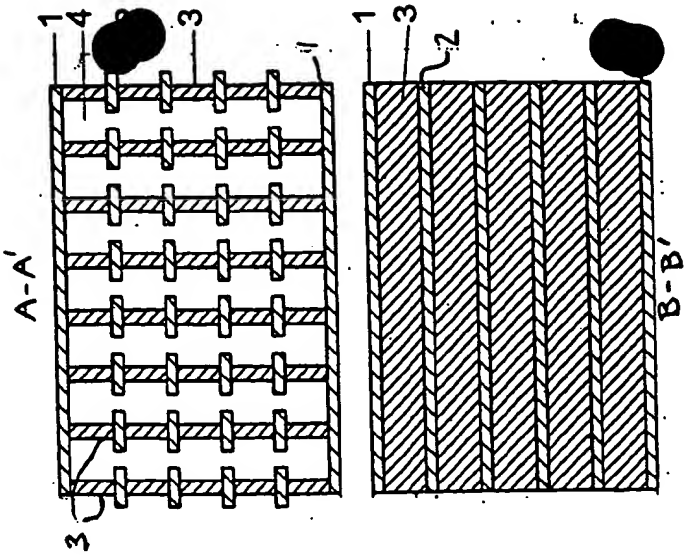

FIG. 3

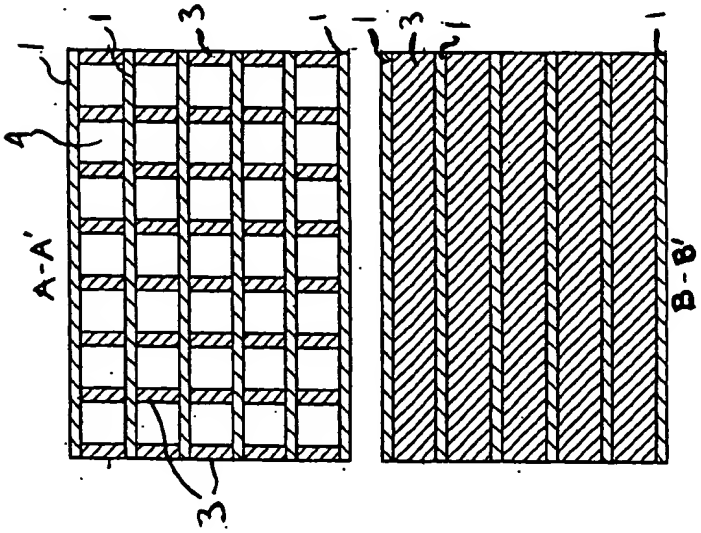

FIG. 2

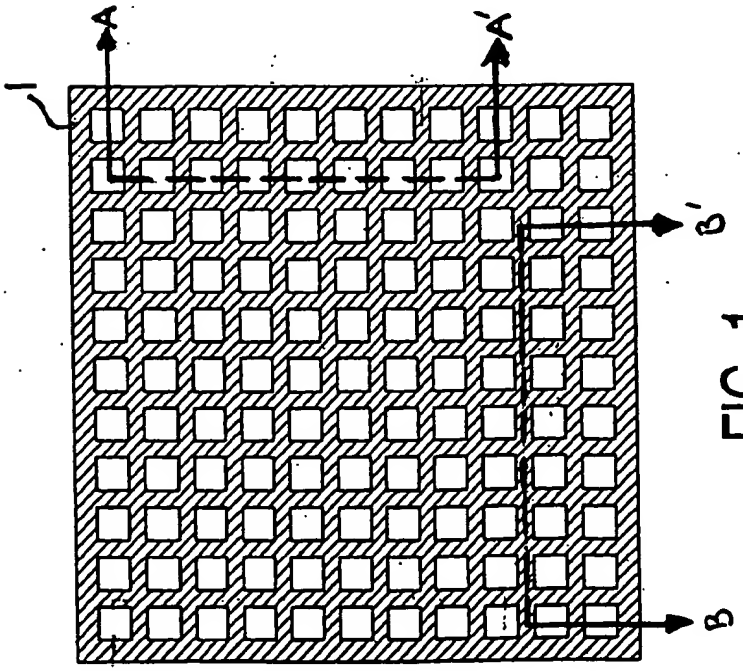

FIG. 1

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Set     Items   Description
S1       4174   BOND()PAD? ?
S2   18402402   UPPER OR LOWER OR FIRST OR SECOND? OR BOTTOM?
S3    8679513   INTERMEDIATE? ? OR INTERMEDIAR???? OR MIDWAY? OR MIDDLE? OR
               TRANSITION? OR HALFWAY?
S4   20298911   LAYER? ? OR SECTION? OR PORTION? OR SEGMENT? OR LEVEL?
S5     979017   DIELECTRIC? OR DIELECT? OR DI()ELECT?
S6      55094   PARALLEL(2N)LINE?
S7    6351623   HOLE? ? OR VOID? OR GAP? OR OPEN???? OR ISOLATE?(2N)AREA?
S8    5098684   S2 AND S4
S9        854   S8 AND S1
S10    558711   S3(6N)S4
S11    464698   S3(3N)S4
S12         0   S9 AND S11 AND S5 AND S6
S13         4   S9 AND S11 AND ( S5 OR S6)
S14         4   RD (unique items)
S15       394   S11 AND T()SHAPE?
S16         2   S5 AND S15
S17         2   RD (unique items)
S18         0   S15 AND S1
S19        18   S9 AND S11
S20        14   S19 NOT S14
S21        14   S20 NOT S17
S22        10   RD (unique items)
S23     58972   VIA(2N)LINE?
S24       148   S23 AND TUNGSTEN?
S25        64   S24 AND (S8 OR S11)
S26        64   RD (unique items)
S27        64   S26 NOT (S13 OR S17 OR S19 OR S22)
S28         1   S27 AND S1
? show files
File   2:INSPEC 1969-2004/Feb W5
         (c) 2004 Institution of Electrical Engineers
File   5:Biosis Previews(R) 1969-2004/Feb W5
         (c) 2004 BIOSIS
File  50:CAB Abstracts 1972-2004/Feb
         (c) 2004 CAB International
File  71:ELSEVIER BIOBASE 1994-2004/Feb W5
         (c) 2004  Elsevier Science B.V.
File 155:MEDLINE(R) 1966-2004/Feb W5
         (c) format only 2004 The Dialog Corp.
File 305:Analytical Abstracts 1980-2004/Jan W4
         (c) 2004 Royal Soc Chemistry
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
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File 347:JAPIO Oct 1976-2003/Oct(Updated 040202)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200415
(c) 2004 Thomson Derwent
File 103:Energy SciTec 1974-2004/Feb B2
(c) 2004 Contains copyrighted material
File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 20
(c) 2004 EBSCO Publishing
File 239:Mathsci 1940-2004/Apr
(c) 2004 American Mathematical Society
File 144:Pascal 1973-2004/Feb W5
(c) 2004 INIST/CNRS
File 399:CA SEARCH(R) 1967-2004/UD=14011
(c) 2004 American Chemical Society
File 25:Weldasearch 1966-2002/Sep
(c) 2004 TWI Ltd
File 95:TEME-Technology & Management 1989-2004/Feb W3
(c) 2004 FIZ TECHNIK
?

14/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014415321 **Image available**
WPI Acc No: 2002-236024/200229
XRPX Acc No: N02-181350
Bond pad **structure fabrication method for integrated circuit, involves forming bond frame comprising island element, with frame element connected to bond frame and covering** bond pad
Patent Assignee: WINBOND ELECTRONICS CORP (WINB-N)
Inventor: LIN S
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6306749	B1	20011023	US 99327874	A	19990608	200229	B
TW 456011	A	20010921	TW 2000111193	A	20000608	200242	

Priority Applications (No Type Date): US 99327874 A 19990608
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6306749	B1			H01L-021/4763	
TW 456011	A			H01L-023/48	

Abstract (Basic): US 6306749 B1
NOVELTY - The method involves forming **bottom dielectric layer** (2) on wafer (1), with underlying polysilicon **layer** (4) formed on top of it. **Middle dielectric layer** (3) is deposited on top of underlying **layer** , and contains at least one through-hole away from area intended to form **bond pad layer** . Through-hole is then filled (24), and metal **bond pad layer** (6) and island element (22) in middle **dielectric** region are formed.
DETAILED DESCRIPTION - Island element is spaced apart from **bond pad layer** and is in contact with underlying **layer** through filled through-hole. A top **dielectric** element is then formed on top of metal bond **layer** , and contains a **second** through-hole which is connected to island element. This hole is filled (23), and subsequently a frame element (21) is formed over top **dielectric layer** , vertically above island element, and overlapping metal bond **layer** . Frame element is connected to island element through filled **second** through-hole.
USE - In semiconductor packaging applications.
ADVANTAGE - The **bond pad** structure manufactured has reduced failure rate due to **bond pad** lift-off problems. This leads to increased production yields and reduced overall production cost, while utilizing existing technology.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic side view showing the **bond pad** side structure.
Wafer (1)
bottom dielectric layer (2)
Middle dielectric layer (3)
Underlying polysilicon **layer** (4)
Metal **bond pad layer** (6)
Frame element (21)
Island element (22)
Through-hole fills (23,24)
DwgNo 4/4
Title Terms: BOND; PAD; STRUCTURE; FABRICATE; METHOD; INTEGRATE; CIRCUIT; FORMING; BOND; FRAME; COMPRISE; ISLAND; ELEMENT; FRAME; ELEMENT; CONNECT; BOND; FRAME; COVER; BOND; PAD

Derwent Class: U11
International Patent Class (Main): H01L-021/4763; H01L-023/48
International Patent Class (Additional): H01L-023/52; H01L-029/40
File Segment: EPI
Manual Codes (EPI/S-X): U11-D03A; U11-D03B

14/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010844039 **Image available**
WPI Acc No: 1996-340992/199634
XRPX Acc No: N96-287067
Capacitive sensor for sensing acceleration forces, esp for direct mounting semiconductor-based sensing elements - has dielectric **insulator disposed between adjacent silicon** layers **to cooperatively form sensing element including mounting surface having conductive contacts formed on them**
Patent Assignee: BREED TECHNOLOGIES INC (BREE-N)
Inventor: BULLIS R H; SWINDAL J L; WIEGAND W J; WINSTON C R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5535626	A	19960716	US 94361277	A	19941221	199634	B

Priority Applications (No Type Date): US 94361277 A 19941221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5535626	A		12	G01P-015/08	

Abstract (Basic): US 5535626 A

The sensor includes a silicon capacitive sensing element (10) comprising three silicon **layers** (12,16,26) having glass **dielectric layers** (14,24) between each pair of silicon **layers** with the **middle** silicon **layer** (16) consisting of a proof mass (18) suspended between the two glass **dielectric layers** by a silicon hinge (20) which is connected to a slightly thicker silicon support **layer** (17) around the periphery between the glass **layers** .

Three metallic **bond pads** (40,42,44) on the surface (45) of the silicon **layers** respectively, are soldered to circuit trace pads (108) on a circuit board (100) which has a glass **upper layer** (104) and a silicon support **layer** (102). The thermal expansion coefficient between the glass **layer** and the sensing element are the same, thereby minimizing thermally induced stresses on the sensing element and the inaccuracies associated with it.

ADVANTAGE - Such direct mounting greatly simplifies mfg. process for such sensors, and eliminates flying leads thereby allowing fabrication of sensing element to much smaller dimensions than in prior art.

Dwg.4/6
Title Terms: CAPACITANCE; SENSE; SENSE; ACCELERATE; FORCE; DIRECT; MOUNT; SEMICONDUCTOR; BASED; SENSE; ELEMENT; **DIELECTRIC** ; INSULATE; DISPOSABLE; ADJACENT; SILICON; **LAYER** ; COOPERATE; FORM; SENSE; ELEMENT; MOUNT; SURFACE; CONDUCTING; CONTACT; FORMING
Derwent Class: S02; U12
International Patent Class (Main): G01P-015/08
File Segment: EPI
Manual Codes (EPI/S-X): S02-G03; S02-K03A1C; U12-B03E

14/9/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010130982 **Image available**
WPI Acc No: 1995-032233/199505
XRPX Acc No: N95-025676

Bare die testing system for silicon integrated circuits - uses low profile connections to and from multilayer interconnection structure and surrounding test circuitry, which do not mechanically interfere with lowering and presenting micro-bump contacts to wafer under test

Patent Assignee: PLESSEY SEMICONDUCTORS LTD (PLES); MITEL SEMICONDUCTOR LTD (MTLC)
Inventor: PEDDER D J

Number of Countries: 009 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2279805	A	19950111	GB 9313721	A	19930702	199505	B
EP 632281	A2	19950104	EP 94304359	A	19940616	199506	
CA 2127234	A	19950103	CA 2127234	A	19940630	199514	
JP 7037948	A	19950207	JP 94171574	A	19940701	199515	
EP 632281	A3	19960717	EP 94304359	A	19940616	199636	
GB 2279805	B	19970917	GB 9313721	A	19930702	199740	
US 5786701	A	19980728	US 94261395	A	19940617	199837	
			US 96625547	A	19960401		

Priority Applications (No Type Date): GB 9313721 A 19930702
Cited Patents: No-SR.Pub; EP 294939; EP 554622; US 5090118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2279805	A		17	H01L-021/66	
EP 632281	A2	E	10	G01R-031/28	
Designated States (Regional): DE FR IT NL SE					
JP 7037948	A		6	H01L-021/66	
US 5786701	A			G01R-031/02	CIP of application US 94261395
CA 2127234	A			H01L-021/66	
EP 632281	A3			H01L-021/66	
GB 2279805	B			H01L-021/66	

Abstract (Basic): GB 2279805 A

The die testing system includes a multilayer interconnection structure in a testing station for bare die. A number of micro-bumps of conductive material are located on interconnection trace terminations. The terminations are distributed in a pattern corresp. to the pattern of contact pads on the die to be tested. The connections to and from the interconnection structure are low profile.

Bond pad connections are used on the substrate periphery at the **level** of the substrate. Low profile ribbon bonding is used between the **bond pads** and the supporting circuit board. The substrate may be silicon or sapphire or other transparent and insulating material. E.g. the total thickness of the multilayer metal and **dielectric** of the substrate is 20 micrometres, while a nickel micro-bump may be 30 micrometres in height. A 10 to 15 micrometre thick, low profile ribbon bond may be used, that does not rise above the allowable 50 micrometre limit.

USE/ADVANTAGE - With multi-chip modules, partly or fully populated; GaAs MMICs. Permits testing of die before separation from wafer.

Dwg.2/6

Abstract (Equivalent): GB 2279805 B

A bare die testing apparatus comprising a multilayer metallisation and **dielectric** structure formed on rigid substrate of electrically insulating material and providing a testing station for bare die, said structure comprising an **upper** metallisation **layer** , a ground plane metallisation **layer** adjacent said substrate, at least one **intermediate** metallisation **layer** , and a plurality of interlayer vias interconnecting at least part of said metallisation **layers** , and providing one or more controlled impedance interconnections adjacent said testing station, said testing station having a plurality of microbumps of conductive material located on interconnection trace terminations of said **upper** metallisation **layer** and distributed in a pattern corresponding to the pattern of contact pads on a bare die to be tested, and connections to and from said multilayer structure, said connections being of **lower** profile than said microbumps to permit testing of a die before separation from a wafer.

Dwg.1

Title Terms: BARE; DIE; TEST; SYSTEM; SILICON; INTEGRATE; CIRCUIT; LOW; PROFILE; CONNECT; MULTILAYER; INTERCONNECT; STRUCTURE; SURROUND; TEST; CIRCUIT; MECHANICAL; INTERFERENCE; **LOWER** ; PRESENT; MICRO; BUMP; CONTACT ; WAFER; TEST
Derwent Class: S01; U11
International Patent Class (Main): G01R-031/02; G01R-031/28; H01L-021/66
International Patent Class (Additional): G01R-031/26
File Segment: EPI
Manual Codes (EPI/S-X): S01-G02B1; U11-F01C1; U11-F01C3; U11-F01D1

14/9/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009255947 **Image available**
WPI Acc No: 1992-383360/199247
XRAM Acc No: C92-170056
XRPX Acc No: N92-292308

Integration of two semiconductor chips inside standard outline package - uses solder bumps on both dice which are bonded face-to-face in lead-on-chip configuration to lead frame

Patent Assignee: GOLDSTAR ELECTRON CO LTD (GLDS); KINSEI ELECTRON KK (KINS-N); GOLDSTAR ELECTRON CO INC (GLDS)
Inventor: CHUN H S
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4215467	A	19921112	DE 4215467	A	19920511	199247	B
JP 5129517	A	19930525	JP 92114940	A	19920507	199325	
KR 9403560	B1	19940423	KR 917632	A	19910511	199605	
US 5572068	A	19961105	US 92861480	A	19920401	199650	
			US 93104244	A	19930809		
			US 94349132	A	19941202		
DE 4215467	C2	20010426	DE 4215467	A	19920511	200124	

Priority Applications (No Type Date): KR 917632 A 19910511
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4215467	A		13	H01L-023/50	
JP 5129517	A		7	H01L-025/065	
KR 9403560	B1			H01L-021/50	
US 5572068	A		14	H01L-023/02	Cont of application US 92861480 Cont of application US 93104244
DE 4215467	C2			H01L-023/50	

Abstract (Basic): DE 4215467 A

The multi-chip package consists of an **upper** and a **lower** semiconductor chip and a leadframe, whereby both chips are electrically connected with lead frame fingers. The chips feature solder-bumps, pref. solder-balls, consisting of an Pb-Sn alloy with, pref. a m.pt. higher than the cure temp. of the epoxy moulding cpd. used to encapsulate the device, on the **bond pads** and attachment to the lead fingers is by soldering.

The solder-bumps are pref. located on the 2 chips along the same longitudinal line and pref. alternating between **upper** and **lower** die. Also claimed is orientation of the bumps on **lower** and **upper** chip along 2 **parallel** longitudinal **lines** and **bond pads** from **upper** and **lower** chips being bonded alternatingly to the lead frame fingers forming 2 comb patterns which are offset from each other by half the pitch between adjacent fingers or with butting lead fingers. An assembly process flow is also claimed.

USE/ADVANTAGE - The process eliminates the wire bonding process, which allows the height above the chips to be reduced and which reduces electrical noise and cross-coupling. The process allows 2 chips to be bonded simultaneously inside a single package, reducing the amount of work required and increasing the density of the device without increasing the package dimensions. Suitable package outlines are Quad flat-pack (QFP), Thin Small Outline Package (TSOP), other SOP and SOJ packages and Mini Square package (MSP).

Dwg.3/4

Abstract (Equivalent): US 5572068 A

A semiconductor package comprising: a. **upper** and **lower** semiconductor chips which include mutually facing active faces, with each of the **upper** and **lower** semiconductor chips having a number of mutually facing pads positioned on **intermediate portions** of the active faces; b. solders formed on the number of pads; c. a number of **first** and a number of **second** connected inner leads alternately arranged and connected to the solders, where each of the **first** connected leads is connected solely to the **upper** semiconductor chip and each of the **second** connected leads is connected solely to the **lower** semiconductor chip, such that the **upper** and **lower** semiconductor chips are electrically connected to the **first** and **second** connected inner leads, respectively.

(Dwg.4/10

Title Terms: INTEGRATE; TWO; SEMICONDUCTOR; CHIP; STANDARD; OUTLINE; PACKAGE; SOLDER; BUMP; DICE; BOND; FACE; FACE; LEAD; CHIP; CONFIGURATION; LEAD; FRAME

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-021/50; H01L-023/02; H01L-023/50; H01L-025/065

International Patent Class (Additional): H01L-021/60; H01L-023/28; H01L-025/07; H01L-025/18

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A05-A01E2; A12-E04; A12-E07C; L04-C24; L04-F05

Manual Codes (EPI/S-X): U11-D01A6; U11-D03C1

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6/9/1 **(Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

014212587 **Image available**
WPI Acc No: 2002-033284/200204
Related WPI Acc No: 1998-398068; 1999-009304; 2003-102345; 2003-729559
XRAM Acc No: C02-009276
XRPX Acc No: N02-025543

Providing of void in spacing between wiring lines of semiconductor substrate, involves depositing conductive layers on the substrate, and subsequently configuring the conductive layers into adjacent wiring lines

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: GIVENS J H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6309946	B1	20011030	US 95550916	A	19951031	200204 B
			US 96723263	A	19960930	
			US 98207890	A	19981208	

Priority Applications (No Type Date): US 95550916 A 19951031; US 96723263 A 19960930; US 98207890 A 19981208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6309946	B1		11	H01L-021/76	Div ex application US 95550916 Cont of application US 96723263 Cont of patent US 5835987

Abstract (Basic): US 6309946 B1

NOVELTY - A void between wiring lines of semiconductor substrate is provided by depositing conductive layers on the substrate; subsequently configuring the conductive layers to adjacent wiring lines; depositing a **dielectric** material on the substrate; and accumulating the **dielectric** material between edges of the extending tops of the wiring lines to seal off an elongated void area.

DETAILED DESCRIPTION - Providing void (32) in a spacing between wiring lines (34, 36, 74, 76) of semiconductor substrate involves depositing at least three conductive layers on the substrate comprising lower, **middle** , and an upper **layer** ; subsequently configuring the conductive layers into at least two adjacent wiring lines, forming the lower and the **middle layers** to each have a lateral width less than a lateral width of the upper layer so that at least two adjacent elongated wiring lines each have a cross-sectional shape of a T, and laterally extending tops on the length of the two adjacent wiring lines; depositing **dielectric** material (86) on the substrate and the semiconductor at least two adjacent elongated wiring lines with the extending tops to form a layer; and causing the **dielectric** material to accumulate between edges of the laterally extending tops of the at least two wiring lines to seal off an elongated void area between the two elongated wiring lines.

USE - For providing void in spacing or for reducing the resistance capacitance (RC) delay between adjacent wiring lines of a semiconductor substrate.

ADVANTAGE - The method minimizes resistance-capacitance coupling. It provides void having low **dielectric** value of 1.0, or reduced line spacing, e.g. less than 1 or less than 0.5 microns. It provides line spacing that is as low as 0.1 microns. The controllably defined void(s) reduce the **dielectric** value in the spacing between adjacent wiring lines, thus reducing RC delay.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the planarized substrate.
Void (32)
Wiring lines (34, 36, 74, 76)
Dielectric material (86)
pp; 11 DwgNo 13/13

Technology Focus:
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The configuring step involves etching by an isotropic overetch process. The lower layer is provided by depositing a barrier layer on the semiconductor substrate and etching the barrier layer using a wet dip process or a reactive ion etching process. The **middle layer** is deposited by etching the conductive layer using wet dip process or reactive ion etching process. The upper layer is deposited by defining a top for the **T shaped** wiring line. The lower layer is etched such that a cross-section of the lower layer is wider than that of the **middle layer** . Under-cuts are defined below the extending tops of the wiring lines. The deposition step is done by chemical vapor deposition. The **dielectric** material is planarized by chemical-mechanical polishing. A plasma enhanced chemical vapor deposition of nitride compound is deposited on the two elongated wiring lines prior to deposition of the **dielectric** material, to serve as an etch-stop layer. At least one via is formed through the **dielectric** material to the etch stop layer, and filling the via with a conductive material. At least one wiring line is connected to an overlying layer through the conductive filled via.
The method also includes defining at least one dimension of the void responsive to the wire line spacing, wire line height, and an extent of the undercuts below the extending tops of at least two adjacent elongated wiring lines. The void provides a **dielectric** constant that is less than that of the **dielectric** material.
INORGANIC CHEMISTRY - Preferred Component: The barrier layer is formed by depositing titanium, titanium nitride, titanium tungsten, or tantalum nitride. The conductive layer comprises aluminum base, a copper base, or a gold base. The upper layer is formed by depositing titanium nitride layer, titanium tungsten layer, titanium layer, titanium aluminide layer, or tantalum nitride layer

Title Terms: VOID; SPACE; WIRE; LINE; SEMICONDUCTOR; SUBSTRATE; DEPOSIT; CONDUCTING; LAYER; SUBSTRATE; SUBSEQUENT; CONDUCTING; LAYER; ADJACENT; WIRE; LINE
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/76
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C10A; L04-C12
Manual Codes (EPI/S-X): U11-C05B9A; U11-C05D3

16/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013085240 **Image available**
WPI Acc No: 2000-257112/200022
XRAM Acc No: C00-078646
XRPX Acc No: N00-191111
Fabrication of high performance metal oxide field effect transistors with an inverted T - shaped gate electrode involves scaling the size of the gate electrode of the transistor
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: FULFORD H J; GARDNER M I; MAY C E
Number of Countries: 021 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200014787	A1	20000316	WO 99US5352	A	19990312	200022	B
US 6090676	A	20000718	US 98149210	A	19980908	200037	
EP 1116267	A1	20010718	EP 99911323	A	19990312	200142	
			WO 99US5352	A	19990312		

Priority Applications (No Type Date): US 98149210 A 19980908
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200014787	A1	E	23	H01L-021/336	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6090676	A			H01L-021/336	
EP 1116267	A1	E		H01L-021/336	Based on patent WO 200014787
Designated States (Regional): DE GB					

Abstract (Basic): WO 200014787 A1

NOVELTY - A high performance metal oxide field effect transistors (MOSFETs) is produced by forming a gate **dielectric** layer on the substrate with a gate electrode (132) formed on the gate **dielectric layer** . **Middle portion** of the gate **dielectric** layer is thicker than the side portions. A dopant is implanted at a first energy level and at a first concentration forming a light doped drain region.

USE - For the fabrication of high performance MOSFETs device.

ADVANTAGE - The process provides a reduced production cost producing a high performance MOSFETs device.

DESCRIPTION OF DRAWING(S) - The drawings show a partial cross-sectional view of a semiconductor structure including a partially oxidized gate electrode, and a partial cross-sectional view of a semiconductor structure undergoing a first implant.

Nitride layer (110)

Gate electrode (132)

pp; 23 DwgNo 4,5a/5

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The gate electrode is a polysilicon material.

Preferred Dopant: The dopant can be an antimony, decaborane ($B_{10}H_6$), arsenic or boron fluoride (BF_2).

ELECTRONICS - Preferred Process: The process further includes oxidizing a portion of the polysilicon gate electrode at the exposed surfaces to a certain depth and removing the oxidized portion of the polysilicon gate electrode leaving the **middle portion** that is thicker than its side portions. The first species of antimony is implanted at an energy level of 5-30 keV with a dose rate of 2E15-6E15 ions/cm2. The second species of antimony is implanted at an energy level of 800-10 keV at a dose rate of 2E15-6E15 ions/cm2.

Title Terms: FABRICATE; HIGH; PERFORMANCE; METAL; OXIDE; FIELD; EFFECT; TRANSISTOR; INVERT; SHAPE; GATE; ELECTRODE; SCALE; SIZE; GATE; ELECTRODE; TRANSISTOR

Derwent Class: L03; U11; U12

International Patent Class (Main): H01L-021/336

International Patent Class (Additional): H01L-021/265; H01L-021/28; H01L-029/423

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C02B; L04-C10B; L04-E01B1

Manual Codes (EPI/S-X): U11-C02A2; U11-C02J6; U11-C05F1; U12-D02A

?

22/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6544512 INSPEC Abstract Number: B2000-05-0170J-010
Title: Reliability of electroless processed thin layered solder joints
Author(s): Wang, L.C.; Mei, Z.; Dauskardt, R.H.
Author Affiliation: Dept. of Mater. Sci. & Eng., Stanford Univ., CA, USA
Conference Title: Materials Reliability in Microelectronics IX. Symposium p.3-8
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 1999 Country of Publication: USA ix+311 pp.
Material Identity Number: XX-1999-03212
Conference Title: Materials Reliability in Microelectronics IX. Symposium
Conference Date: 6-8 April 1999 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: There has recently been an increasing interest in using electroless processes to produce the metal thin film stacks that make up the **bond pads** in solder ball grid array (BGA) packages. Electroless processes produce a more uniform and better controlled film thickness, but the resulting metal stacks have exhibited less mechanical reliability than that of traditional electrolytic stacks. This paper addresses a layered system consisting of a eutectic Sn-Pb solder sandwiched between stacks of Cu, Ni, and Au thin films. The samples were tested to determine cyclic fatigue behavior and fracture toughness values using traditional linear elastic fracture mechanics techniques. Surprisingly, fatigue crack propagation occurred in the **middle** of the solder **layer** , even though the electroless interface was expected to be very weak. In contrast, fracture tests did appear to cause failure near an interface, but not necessarily at the electroless interface. Fracture toughness values measured for these samples were much **lower** than those reported for bulk metals. These results are discussed in terms of the microstructures present in order to determine possible relationships between the microstructure of the solder joint and its fracture behavior. (4 Refs)
Subfile: B
Descriptors: ball grid arrays; copper; electroless deposition; fatigue; fracture mechanics; fracture toughness; gold; integrated circuit bonding; integrated circuit interconnections; integrated circuit packaging; integrated circuit reliability; lead alloys; microassembling; nickel; reflow soldering; tin alloys
Identifiers: reliability; electroless processed thin layered solder joints; electroless processes; metal thin film stacks; **bond pads** ; solder BGA packages; solder ball grid array packages; film thickness; metal stacks; mechanical reliability; electrolytic stacks; eutectic Sn-Pb solder; Cu-Ni-Au thin film stacks; cyclic fatigue behavior; fracture toughness; linear elastic fracture mechanics; fatigue crack propagation; solder **layer** ; electroless interface; fracture tests; interface failure; microstructures ; solder joint microstructure; SnPb-Au-Ni-Cu
Class Codes: B0170J (Product packaging); B2570 (Semiconductor integrated circuits); B0170N (Reliability); B2240 (Microassembly techniques); B0170G (General fabrication techniques); B0520J (Deposition from liquid phases)
Chemical Indexing:
SnPb-Au-Ni-Cu int - SnPb int - Au int - Cu int - Ni int - Pb int - Sn int - SnPb bin - Pb bin - Sn bin - Au el - Cu el - Ni el (Elements - 2,1,1,1,5)

22/9/2 (Item 2 from file: 2)

6155268 INSPEC Abstract Number: B1999-03-0170J-036

Title: Maskless, direct deposition of copper onto aluminum bond pads **for flip chip applications**

Author(s): Fang, M.; O'Keefe, T.; Stroder, M.; Shih, W.; O'Keefe, M.; Strawser, R.; Via, D.
Author Affiliation: Missouri Univ., Rolla, MO, USA

Conference Title: Electronic Packaging Materials Science X. Symposium p.85-90
Editor(s): Belton, D.J.; Gaynes, M.; Jacobs, E.G.; Pearson, R.; Wu, T.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 1998 Country of Publication: USA ix+262 pp.
ISBN: 1 55899 421 1 Material Identity Number: XX-1998-03239
Conference Title: Electronic Packaging Materials Science X. Symposium
Conference Date: 14-16 April 1998 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); New Developments (N); Practical (P); Experimental (X)

Abstract: Flip chip interconnection of integrated circuits (IC) for packaging applications such as direct chip attachment use Pb-Sn solders as the connection between the die and the substrate. Underbump metallization is typically used as a transition from the nonsolderable Al **bond pad** on the IC to a solderable surface such as copper using traditional blanket metal deposition, photolithography and etching procedures. In this study, we report for the **first** time the use of a novel process for selective deposition of adherent copper directly on to aluminum thin films, eliminating the need for adhesion promoting **transition layers** and additional patterning steps. Using copper bearing organic solutions and standard electroless and electrolytic copper plating baths, as-deposited and annealed sputter deposited Al-x%Cu (x=0 to 2) thin films were coated with metallic copper. An increase in the organically deposited copper nucleation site density was observed with increasing copper concentration in the sputtered aluminum/copper thin films. Preliminary results using focused ion beam microscopy indicated that dissolution of the aluminum oxide surface and subsequent deposition of copper by cementation occurs in the nonconducting organic solution at sub-micron reaction lengths. Qualitative adhesion testing of samples resulted in the majority of films passing the tape test. Demonstration of the process using 50 mu m diameter vias in BCB coated flip chip test vehicles from MCNC are presented. (2 Refs)

Subfile: B
Descriptors: adhesion; copper; dissolving; electrodeposition; electroless deposition; flip-chip devices; focused ion beam technology; integrated circuit interconnections; integrated circuit metallisation; integrated circuit packaging; integrated circuit testing; ion microscopy; microassembling; nucleation; soldering
Identifiers: Cu maskless direct deposition; aluminum **bond pads** ; flip chip applications; flip chip interconnection; integrated circuits; IC packaging; direct chip attachment; Pb-Sn solders; die-substrate connection; underbump metallization; nonsolderable Al **bond pad** ; solderable surface; blanket metal deposition; photolithography; etching; selective Cu deposition; aluminum thin films; adhesion promoting **transition layers** ; patterning; copper bearing organic solutions; electrolytic copper plating baths; electroless copper plating baths; annealed sputter deposited Al-Cu thin films; as-deposited sputter deposited Al-Cu thin films; organically deposited copper nucleation site density; copper concentration; sputtered aluminum/copper thin films; focused ion beam microscopy; aluminum oxide surface dissolution; cementation; nonconducting organic solution; reaction

length; adhesion testing; tape test; via diameter; BCB coated flip chip test vehicles; 50 micron; SnPb-Cu-AlCu; AlCu; Al
Class Codes: B0170J (Product packaging); B2550F (Metallisation and interconnection technology); B2240 (Microassembly techniques); B0520J (Deposition from liquid phases); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); B0170G (General fabrication techniques)
Chemical Indexing:
SnPb-Cu-AlCu int - AlCu int - SnPb int - Al int - Cu int - Pb int - Sn int - AlCu bin - SnPb bin - Al bin - Cu bin - Pb bin - Sn bin - Cu el (Elements - 2,1,2,4)
AlCu sur - Al sur - Cu sur - AlCu bin - Al bin - Cu bin (Elements - 2)
Al sur - Al el (Elements - 1)
Numerical Indexing: size 5.0E-05 m

22/9/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015939498 **Image available**
WPI Acc No: 2004-097339/200410
XRAM Acc No: C04-040411
XRPX Acc No: N04-077507
Selective formation of metal feature on intermediate structure of semiconductor device, comprises selectively forming metal feature on first exposed metal structure, without forming metal of metal feature on second exposed metal structure
Patent Assignee: GLEASON J N (GLEA-I)
Inventor: GLEASON J N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030219976	A1	20031127	US 2002154755	A	20020524	200410	B

Priority Applications (No Type Date): US 2002154755 A 20020524
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030219976	A1		8	H01L-023/58	

Abstract (Basic): US 20030219976 A1
NOVELTY - A metal feature is selectively formed on an intermediate structure of a semiconductor device, by providing the intermediate structure comprising a **first** and a **second** exposed metal structure; and selectively forming the metal feature on the **first** exposed metal structure, without forming a metal of the metal feature on the **second** exposed metal structure.
USE - Used for the selective formation of a metal feature, i.e. interconnect cap, redistribution **layer** , **bond pad** , or preferably metal **layer** , on an **intermediate** structure of a semiconductor device, i.e. static random access memory or a FLASH memory chip (claimed).
ADVANTAGE - The metal feature is formed on the **first** exposed metal structure, without any metal of the metal feature being formed on the **second** exposed metal structure.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic representation of a semiconductor wafer.
Semiconductor wafer (2)
Bond pad (4)

Fuse (6)
pp; 8 DwgNo 1a/1
Technology Focus:
TECHNOLOGY FOCUS - METALLURGY - Preferred Process: The process comprises providing the intermediate structure comprising a **bond pad** (s) (4) as the **first** exposed metal structure, and an opened fuse(s) (6) as the **second** exposed metal structure; and forming the metal feature on the **bond pad** (s) without reforming the opened fuse(s). Selective formation of the metal feature on the **first** exposed metal structure comprises electrolessly plating the metal feature on the **first** exposed metal structure; adjusting a concentration of stabilizer in an electroless plating solution; forming the metal feature after probe testing of the intermediate structure of the semiconductor device; and electrolessly plating the metal feature from a metal comprising palladium, gold, tin, silver, copper, or preferably nickel. Determining whether the metal feature is selectively plated on the **first** metal structure, comprises viewing the **first** metal structure and the opened fuse(s), by scanning electron microscopy to determine whether a metal of the metal feature is deposited on the opened fuse(s).

Preferred Parameter: Increasing the concentration of the stabilizer decreases a critical size of the **first** metal structure, and decreases a size of the metal feature. Decreasing the concentration of stabilizer increases a critical size of the **first** metal structure, and increases a size of the metal feature.

INORGANIC CHEMISTRY - Preferred Material: The stabilizer is from compounds of group VI elements comprising compounds of sulfur, selenium, or tellurium; compounds comprising oxygen comprising arsenic oxide, iodine oxide, or molybdenum oxide; heavy metal cations comprising tin, lead, mercury, or antimony; or unsaturated organic acids comprising maleic acid or itaconic acid
Title Terms: SELECT; FORMATION; METAL; FEATURE; INTERMEDIATE; STRUCTURE; SEMICONDUCTOR; DEVICE; COMPRISE; SELECT; FORMING; METAL; FEATURE; **FIRST** ; EXPOSE; METAL; STRUCTURE; FORMING; METAL; METAL; FEATURE; **SECOND** ; EXPOSE; METAL; STRUCTURE
Derwent Class: L03; U11; U13
International Patent Class (Main): H01L-023/58
International Patent Class (Additional): H01L-021/44
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C10
Manual Codes (EPI/S-X): U11-C05E; U11-D01C9; U13-C04B1

22/9/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015693002 **Image available**
WPI Acc No: 2003-755191/200371
Related WPI Acc No: 2002-617214; 2003-491671
XRAM Acc No: C03-207200
XRPX Acc No: N03-605064
Substrate for semiconductor assemblies, has wetting agent layer **provided on** portion **of surface, to promote adhesion of adhesive** layer **used to attach semiconductor die to** portion **of substrate surface**
Patent Assignee: DICKEY B L (DICK-I); JIANG T (JIAN-I)
Inventor: DICKEY B L; JIANG T
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week

US 20030094690 A1 20030522 US 2000591144 A 20000609 200371 B
US 2002334230 A 20021230

Priority Applications (No Type Date): US 2000591144 A 20000609; US 2002334230 A 20021230
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030094690	A1		9	H01L-023/14	Cont of application US 2000591144 Cont of patent US 6501170

Abstract (Basic): US 20030094690 A1

NOVELTY - A substrate (104) has a wetting agent **layer** provided on a **portion** of a substrate surface, to promote adhesion of an adhesive **layer** which is used to attach a semiconductor die (102) to a **portion** of the substrate surface.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor assembly (100), which comprises a substrate having a front surface and a back surface (114), semiconductor die(s) having an active surface (112) provided with several **bond pads** (134), and at least one semiconductor die is adhesively secured to a **portion** of front or back surface of the substrate by an adhesive **layer** , a wire bond(s) extending from **bond pad** (s) of semiconductor die to a **portion** of front or back surface of the substrate, and a wetting agent **layer** provided on at least one **portion** of active surface of semiconductor die or **portion** of front surface or back surface of substrate to which the semiconductor die is secured.

USE - For semiconductor assemblies, such as wire bonding chip-on-board semiconductor assemblies (both claimed).

ADVANTAGE - The substrate has a wetting agent **layer** which interacts with the adhesive of adhesive tape when heated. Consequently, adhesion of adhesive tape between a semiconductor die and substrate, or bonding between multiple substrates and/or multiple semiconductor devices is enhanced, and the adhesive tape is bonded at **lower** temperature. The bonding of adhesive tape at **lower** temperature decreases the thermal stress between the semiconductor die and the substrate, and the potential for out-gassing from the adhesive during ball grid array attachment adhered of the substrate and semiconductor die to another substrate. The substrate is adhered to semiconductor die in a cost-effective and efficient way.

DESCRIPTION OF DRAWING(S) - The figure shows cross- **sectional** side view of **intermediate** semiconductor assembly.

semiconductor assembly (100)
semiconductor die (102)
substrate (104)
adhesive tape (108)
active surface of semiconductor die (112)
back surface of substrate (114)
bond pads (134)
pp; 9 DwgNo 1/6

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred **Layer** : The wetting agent **layer** comprises one or several **layers** , and covers at least a **portion** of substrate surface. The wetting agent **layer** comprises silane coupling agent, titanate coupling agent, and/or a solvent base.

Preferred Property: The wetting agent **layer** interacts with adhesive(s) on the adhesive tape when the substrate is heated to a predetermined temperature.

POLYMERS - Preferred Substrate: The substrate is bismaleimide triazine substrate, FR-4 (sic) printed circuit board, ceramic substrate

and/or polyimide substrate.

ELECTRONICS - Preferred Arrangement: An adhesive tape comprising an adhesive(s) and having adhesive coating on sides (I and II), is interposed between substrate surface and surface of semiconductor die, and attaches the substrate to semiconductor die.

Preferred Semiconductor Assembly: The semiconductor assembly is chip-on-board semiconductor assembly having wire bonds or tape-automated-bonding connection

Title Terms: SUBSTRATE; SEMICONDUCTOR; ASSEMBLE; WET; AGENT; **LAYER** ; **PORTION** ; SURFACE; PROMOTE; ADHESIVE; ADHESIVE; **LAYER** ; ATTACH; SEMICONDUCTOR; DIE; **PORTION** ; SUBSTRATE; SURFACE

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-023/14

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A08-S05; A12-E07C; L04-C17D

Manual Codes (EPI/S-X): U11-E02A2; U11-E02A3

Polymer Indexing (PS):

<01>

001 018; P1081-R F72 D01

002 018; ND01; K9416; Q9999 Q7476 Q7330; K9483-R; K9676-R; B9999 B5301 B5298 B5276

22/9/5 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015543502 **Image available**

WPI Acc No: 2003-605658/200357

Related WPI Acc No: 2001-201282; 2001-233706; 2002-582118; 2003-876085

XRPX Acc No: N03-482843

Semiconductor device package assembly e.g. for dynamic random access memory, has retainer holding semiconductor device in preset relation with substrate and wire bond connection between lead of lead frame and pad

Patent Assignee: CORISIS D J (CORI-I); KEETH B (KEET-I); MICRON TECHNOLOGY INC (MICR-N)

Inventor: CORISIS D J; KEETH B

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020074629	A1	20020620	US 97784362	A	19970117	200357 B
			US 971638	A	19971231	
			US 99472291	A	19991227	
			US 200271943	A	20020205	
US 6580158	B2	20030617	US 97784362	A	19970117	200357
			US 971638	A	19971231	
			US 99472291	A	19991227	
			US 200271943	A	20020205	

Priority Applications (No Type Date): US 97784362 A 19970117; US 971638 A 19971231; US 99472291 A 19991227; US 200271943 A 20020205

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020074629	A1		22	H01L-023/495	Div ex application US 97784362 Cont of application US 971638 Cont of application US 99472291
US 6580158	B2			H01L-023/495	Div ex application US 97784362 Cont of application US 971638 Cont of application US 99472291 Div ex patent US 6103547 Cont of patent US 6133622

Abstract (Basic): US 20020074629 A1
NOVELTY - The semiconductor package assembly comprises:
(i) a substrate;
(ii) a semiconductor device positioned on the substrate having an active surface and at least one **bond pad** ;
(iii) an insulation material covering a **portion** of the active surface having tape with adhesive **layer** ;
(iv) a semiconductor device retainer having **portions** engaging **portions** on the **first** and **second** sides of the substrate, and **portion** engaging a **portion** of the tape on active surface of semiconductor device;
(v) a lead frame having at one lead;
(vi) at least one electrical connection between at least one lead of lead frame and at least one **bond pad** .
USE - Semiconductor device package assembly e.g. for dynamic random access memory, has retainer holding semiconductor device in preset relation with substrate and wire bond connection.
ADVANTAGE - Reduces lead inductance in IC packages.
DESCRIPTION OF DRAWING(S) - The drawing shows a side view of one side of the retainer mounted in a vertical surface mount package.
(1) **first** side;
(10) IC package;
(12) substrate;
(14) semiconductor device;
(16) insulating tape;
(18) retainer;
(20) lead frame;
(22) wire bond interconnections;
(24) **bond pads** ;
(52) **second** leads;
(54) third leads;
(56,66) **first portion** ;
(58,68) **second transition portion** ;
(60,70) third semiconductor device **portion** ;
(62) slotted opening.
pp; 22 DwgNo 1/11
Title Terms: SEMICONDUCTOR; DEVICE; PACKAGE; ASSEMBLE; DYNAMIC; RANDOM; ACCESS; MEMORY; RETAIN; HOLD; SEMICONDUCTOR; DEVICE; PRESET; RELATED; SUBSTRATE; WIRE; BOND; CONNECT; LEAD; LEAD; FRAME; PAD
Derwent Class: U11
International Patent Class (Main): H01L-023/495
File Segment: EPI
Manual Codes (EPI/S-X): U11-D03A1; U11-D03A6

22/9/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015369814 **Image available**
WPI Acc No: 2003-430752/200340
XRAM Acc No: C03-113991
XRPX Acc No: N03-343838
Micro-machined device for controllably directing beam of light has mirror coupled to support structure by pair of single-gimbaled dual-axis hinges to provide rotational movement of the mass about two axes of rotation
Patent Assignee: INPUT/OUTPUT INC (INPU-N)
Inventor: GOLDBERG H; SELVAKUMAR A; YI T; YU D

Number of Countries: 100 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200340801	A1	20030515	WO 2002US33290	A	20021018	200340 B
US 20030118277	A1	20030626	US 2001348083	P	20011019	200343
			US 2001345919	P	20011109	
			US 2002273628	A	20021018	

Priority Applications (No Type Date): US 2001345919 P 20011109; US 2001348083 P 20011019; US 2002273628 A 20021018
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200340801	A1	E	49	G02B-026/08	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

US 20030118277 A1 G02B-006/26 Provisional application US 2001348083
Provisional application US 2001345919

Abstract (Basic): WO 200340801 A1

NOVELTY - Micro-machined device for controllably directing a beam of light has a mirror coupled to a support structure by a pair of single-gimbaled dual-axis hinges to provide rotational movement of the mass about two axes of rotation, a top cap having a window to allow light to reach the mirror, a 1bottom cap bonded to the mirror support structure, and electrodes disposed on the top and/or **bottom** cap(s).

DETAILED DESCRIPTION - Micro-machined device for controllably directing a beam of light comprises a mirror (112) coupled to a support structure by a pair of single-gimbaled dual-axis hinges to provide rotational movement of the mass about two axes of rotation, a top cap (110) bonded to the mirror support structure and having a window to allow light to reach the mirror, a **bottom** cap (114) bonded to the mirror support structure, and electrodes disposed on the top and/or **bottom** cap(s). The electrodes when energized with electrical energy provide a selectable force to the mirror for moving the mirror in angular directions. The mirror includes at least one **portion** contacting at least one of the top and **bottom** caps during angular movement to stop movement of the mirror, such that the mirror position is one of discrete predetermined angular positions.

An INDEPENDENT CLAIM is also included for a planar fabrication method for creating a multi-tiered micro-machined device having at least three tiers, which comprises: fabricating a **first** wafer tier having at least one electrically conductive **first** lead responsive to electrical energy applied to the **first** leads; fabricating a **second** wafer tier having at least one electrically conductive **second** lead responsive to electrical energy applied to the **second** leads; fabricating a middle wafer tier including a **first** electrically conductive **portion** and a **second** electrically conductive **portion** ; and coupling the **middle** wafer tier between the **first** and **second** wafer tiers.

USE - The micro-machined device is used for controllably directing a beam of light.

ADVANTAGE - Manufacturing personnel or machinery are allowed access to the several **bond pads** via multiple electrical conduits located on various wafers of the three-wafer stack. The need for complicated

through-wafer via fabrication is obviated, and a planar machining process to fabricate the multi-tier micro-electromechanical system structure is provided.

DESCRIPTION OF DRAWING(S) - The figure is an exploded view of a micro-electromechanical systems mirror assembly.

Top cap (110)

Mirror (112)

Bottom cap (114)

pp; 49 DwgNo 1C/12

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Device: The device further comprises an overlay coupled to the top cap and including ports for allowing light to pass through the overlay, optic fibers for directing light into and from the device and coupled to the ports for directing light, and a movement control structure disposed on the **bottom** cap to control movement of the mirror. The mirror further comprises a **layer** of material on a surface opposite the mirror surface. The material is selected to balance stress across the mirror to reduce mirror bowing.

Preferred Method: Fabrication of the middle wafer further comprises fabricating a movable micro structure on a **portion** of the **middle** wafer. The method further comprises forming a recess in each of the **first** and **second** wafers to allow movement of the micro structure, and forming a movement-control structure in the **first** wafer recess to control movement of the micro structure.

Fabricating the **first** wafer includes etching a **portion** of the **first** wafer substrate to form a **first** recess having a movement-control structure and depositing metal in at least the **first** recess to form **first** wafer electrodes. Fabricating the **second** wafer includes etching a **portion** of the **second** wafer substrate to form a **second** recess and depositing metal on at least one surface of the **second** wafer to form **second** wafer electrodes, and fabricating the middle wafer includes forming a gimbaled microstructure movable in the **first** and **second** recesses when energy is applied to the **first** and **second** electrodes.

Title Terms: MICRO; MACHINING; DEVICE; CONTROL; DIRECT; BEAM; LIGHT; MIRROR ; COUPLE; SUPPORT; STRUCTURE; PAIR; SINGLE; DUAL; AXIS; HINGE; ROTATING; MOVEMENT; MASS; TWO; AXIS; ROTATING

Derwent Class: L03; P81; V06; V07

International Patent Class (Main): G02B-006/26; G02B-026/08

International Patent Class (Additional): G02B-006/42

File Segment: CPI; EPI; EngPI

Manual Codes (CPI/A-N): L03-G02

Manual Codes (EPI/S-X): V06-M06G; V06-N22; V06-U14; V07-K

22/9/7 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014394960 **Image available**

WPI Acc No: 2002-215663/200227

Related WPI Acc No: 2003-659772; 2003-719799

XRAM Acc No: C02-065866

XRPX Acc No: N02-165208

Microelectronic device for coupling semiconductor die to die terminals, includes elongated lead which comprises bonding portion **, terminal** portion **and narrow** intermediate portion

Patent Assignee: ALLEN T J (ALLE-I); BROOKS J M (BROO-I); KINSMAN L D (KINS-I); MA M K F (MAMK-I); SCHOENFELD A (SCHO-I); MICRON TECHNOLOGY INC

(MICR-N)
Inventor: ALLEN T J; BROOKS J M; KINSMAN L D; MA M K F; SCHOENFELD A
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010052638	A1	20011220	US 9854275	A	19980402	200227 B
			US 2001932080	A	20010817	
US 6579746	B2	20030617	US 9854275	A	19980402	200341
			US 2001932080	A	20010817	

Priority Applications (No Type Date): US 9854275 A 19980402; US 2001932080 A 20010817
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010052638	A1		19	H01L-023/495	Div ex application US 9854275
US 6579746	B2			H01L-021/44	Div ex application US 9854275

Abstract (Basic): US 20010052638 A1

NOVELTY - A microelectronic device comprises a semiconductor die (120) having die terminal(s) (121); and an elongated lead (140) comprising a bonding **portion** (142), a terminal **portion** (143) and an **intermediate portion** (144). The width of the **intermediate portion** of the lead is less than that of the bonding **portion** .

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (A) a computer system, comprising:

(a) a data input device,

(b) a data output device and

(c) the above microelectronic device coupled to the data input and output devices; (B) a method for coupling a **first** and a **second** lead to a **first** and a **second** die terminal, respectively; and (C) a method for selecting the impedance/capacitance of a conductive path between a die terminal and a terminal of a die package.

USE - For coupling a semiconductor die to die terminals.

ADVANTAGE - The inventive microelectronic device allows for increased number of leads to be positioned on the die compared to conventional die packages, because the leads may be spaced more closely together. It may have a reduced overall size and capacitance, and a faster signal transmission to and/or from the **bond pads** .

DESCRIPTION OF DRAWING(S) - The figure is a partially broken top plan view of a die package having staggered leads extending over a surface of a semiconductor die.

Die package (110)
Die (120)
Die terminals (121)
Leads (140)
Bonding **portion** (142)
Terminal **portion** (143)
Intermediate portion (144)
Conductive couplers (150)
pp; 19 DwgNo 3/12

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The lead is affixed to the die with at least its bonding **portion** engaging a surface of the die proximate the edge. The die terminal is a solder ball which is engaged with the bonding **portion** of the lead. A conductive coupler (150), preferably a gold wire, an aluminum wire and/or a conductive adhesive, is coupled to the die terminal at one end and to the bonding **portion** of the lead at the other end. The die is attached to a printed circuit board, and is surrounded by an encapsulating material to form a package (110). The sizes and shapes of

the lead and of the conductive coupler are selected to produce a low total capacitance and a high overall inductance.

METALLURGY - Preferred Material: The lead is made from a copper alloy and/or from a nickel/iron alloy

Title Terms: MICROELECTRONIC; DEVICE; COUPLE; SEMICONDUCTOR; DIE; DIE; TERMINAL; ELONGATE; LEAD; COMPRISE; BOND; **PORTION** ; TERMINAL; **PORTION** ; NARROW; INTERMEDIATE; **PORTION**
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/44; H01L-023/495
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C24
Manual Codes (EPI/S-X): U11-D03A2; U11-D03B1; U11-E02A3

22/9/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013376781 **Image available**
WPI Acc No: 2000-548719/200050
XRAM Acc No: C00-163707
XRPX Acc No: N00-405975

Integrated circuit package to be attached to an organic substrate e.g. printed circuit board has a semiconductor die, an organic structure, and an adhesive tape

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: JIANG T; SCHROCK E A
Number of Countries: 090 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200042648	A1	20000720	WO 2000US687	A	20000111	200050	B
AU 200027244	A	20000801	AU 200027244	A	20000111	200054	
US 6541872	B1	20030401	US 99227942	A	19990111	200324	

Priority Applications (No Type Date): US 99227942 A 19990111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200042648	A1	E	33	H01L-021/58	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

AU 200027244	A		Based on patent WO 200042648
US 6541872	B1	H01L-023/48	

Abstract (Basic): WO 200042648 A1

NOVELTY - An integrated circuit package has a semiconductor die, an organic structure, and an adhesive tape that is disposed between the organic support structure and the semiconductor die. The adhesive tape has adhesive(s) consisting of pressure sensitive, thermoplastic, or thermoset adhesives.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(A) a system comprising a processor, and a memory device that is coupled to the processor; and

(B) a method for fabricating a semiconductor die (10) to an organic support comprising selecting two-sided adhesive tape (40) consisting of pressure sensitive, thermoplastic, or thermoset adhesives.

A **first** side (24) of this tape is affixed to a surface of the organic support structure. The face of the semiconductor die is then

affixed to the **second** side (28) of the adhesive tape.

USE - To be attached directly to an organic substrate e.g. PCB.

ADVANTAGE - The invention provides packages that are smaller and are more economical to produce than conventional encapsulated packages. The tape, used to mount the die to the substrate, eliminates resin bleeding, improves bond line control with less face damage to glob-top filler particles, broaden selection of available fillers, while improving in-line processing.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged side view of the semiconductor package.

Semiconductor die (10)
PCB substrate (12)
Die face (14)
Bond pads (16)
First side (24)
Second side (28)
Lead connection pads (30)
Aperture (32)
Bond wires (38)
Adhesive tape (40)
pp; 33 DwgNo 1/6

Technology Focus:

TECHNOLOGY FOCUS - POLYMERS - Preferred Conditions: The adhesive tape is a multiple layered adhesive, which has a **first** and **second layers** that are adjacent to the organic support i.e. a printed circuit board (PCB) substrate (12), and the semiconductor die, respectively, and a carrier **layer** that is **intermediate** the **first** and the **second layer** . The **first** and **second** adhesive **layers** have coefficients of thermal expansion that are identical to the structures they are adjacent with. These are comprised of a (pressure activated) thermoset or thermoplastic while the carrier **layer** is of a polyimide film.

Extension Abstract:

EXAMPLE - In an EMBODIMENT of the method, **bond pads** (16) are electrically connected to the lead connection pads (30) having bond wires (38) that pass through an aperture (32). An encapsulating material having a curable glob-top that is formed of a viscous material, is formed around the **portions** of the die and the organic support to encapsulate the **bond pads** , bond wires, lead connections, and the **portion** of the die face (14) and the support structure. The organic support is then inverted and a **second** curable glob-top is then applied to a backside of the semiconductor die. The die and the organic support are then cured followed by trimming the organic support to form a ball-grid-array (BGA) package, which is electrically interconnected to a receiver.

Title Terms: INTEGRATE; CIRCUIT; PACKAGE; ATTACH; ORGANIC; SUBSTRATE; PRINT ; CIRCUIT; BOARD; SEMICONDUCTOR; DIE; ORGANIC; STRUCTURE; ADHESIVE; TAPE
Derwent Class: A26; A85; G03; L03; U11
International Patent Class (Main): H01L-021/58; H01L-023/48
File Segment: CPI; EPI
Manual Codes (CPI/A-N): A12-E07C; G03-B04; L04-C21; L04-C26
Manual Codes (EPI/S-X): U11-E02A3
Polymer Indexing (PS):
<01>
001 018; P1081-R F72 D01; H0317; H0328; S9999 S1285-R; S9999 S1650 S1649
002 018; Q9999 Q7476 Q7330; K9416; ND01; K9574 K9483; K9676-R; Q9999 Q6633
<02>
001 018; P0000

002 018; Q9999 Q7476 Q7330; K9416; ND01; K9574 K9483; K9676-R; Q9999-Q6633; Q9999 Q6644-R; Q9999 Q6677 Q6644

22/9/9 **(Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

013312900 **Image available**
WPI Acc No: 2000-484837/200043
XRPX Acc No: N00-360501

Circuit board assembly for accommodating fine pitch applications

Patent Assignee: FORD MOTOR CO (FORD)
Inventor: GOENKA L N
Number of Countries: 026 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1026928	A2	20000809	EP 2000300553	A	20000126	200043	B
US 6111204	A	20000829	US 99246864	A	19990208	200043	

Priority Applications (No Type Date): US 99246864 A 19990208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1026928	A2	E	8	H05K-001/11	
US 6111204	A			H05K-001/09	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Abstract (Basic): EP 1026928 A2

NOVELTY - The assembly includes an electrically insulative substrate surface (10). Several tri-metal- **layer bond pads** (12) are arranged in a straight row on the substrate surface. The row defines a width direction. Each **bond pad** includes a **bottom layer** (14) attached to the substrate surface. A top **layer** (18) is disposed above and concentric with the **bottom layer** . Both the **bottom** and top **layers** are made of the same **first** metal, the top **layer** being larger than the **bottom layer** for at least two adjacent **bond pads** . A **middle layer** (16) is made of a **second** metal connecting the **bottom** and top **layers** .

A circuit trace (20) on the substrate surface is made of the **first** metal. The circuit trace runs between two adjacent tri-metal- **layer bond pads** .

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for an etched tri-metal- **layer** circuit board and for an air bridge circuit board assembly.

USE - For **bond pads** for fine-pitch application on air bridge circuit boards.

ADVANTAGE - Special shaping of **bond pads** enables circuit trace to be spaced closely to **bottom layers** of adjacent **bond pads** , while allowing top **layers** of pads to be made much larger to avoid delamination by associated **middle layers** .

DESCRIPTION OF DRAWING(S) - The figure shows top and side views of ETM circuit **bond pads** for a fine-pitch application.

Substrate surface (10)
Tri-metal- **layer bond pads** (12)
Bottom layer (14)
Middle layer (16)
Top **layer** . (18)
pp; 8 DwgNo 7,8/12

Title Terms: CIRCUIT; BOARD; ASSEMBLE; ACCOMMODATE; FINE; PITCH; APPLY

Derwent Class: V04
International Patent Class (Main): H05K-001/09; H05K-001/11
File Segment: EPI
Manual Codes (EPI/S-X): V04-Q01; V04-Q05

22/9/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010672825 **Image available**
WPI Acc No: 1996-169779/199617
Lead on chip package - has double-sided adhesive tape attached to bottom of lead frame with extended leads and middle of die with bonding pads to wire-bond lead extension and corresponding bonding pad
Patent Assignee: HYUNDAI ELECTRONICS CO LTD (HYUN-N)
Inventor: KONG B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 9406581	B1	19940722	KR 9119552	A	19911105	199617	B

Priority Applications (No Type Date): KR 9119552 A 19911105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 9406581	B1		1	H01L-023/04	

Abstract (Basic): KR 9406581 B
The package includes a lead frame (20) with an extension (E) of the leads (22). A double-sided adhesive tape (26) is attached to the **bottom** of the lead frame corresponding to the extended lead **portion**. A die (24) has its **middle portion** corresponding to the adhesive tape with bonding pads (24A) formed on its outer face. One side of the adhesive tape is attached to the **bottom** of the lead extension. The **middle portion** (A) of the die is attached to the other side of the adhesive tape to wire-bond the lead extension and corresponding bonding pad by the **bond pad**.
Dwg.1/1
Title Terms: LEAD; CHIP; PACKAGE; DOUBLE; SIDE; ADHESIVE; TAPE; ATTACH; **BOTTOM**; LEAD; FRAME; EXTEND; LEAD; MIDDLE; DIE; BOND; PAD; WIRE; BOND; LEAD; EXTEND; CORRESPOND; BOND; PAD
Derwent Class: U11
International Patent Class (Main): H01L-023/04
File Segment: EPI
Manual Codes (EPI/S-X): U11-D03A1B; U11-E01B
?

27/9/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015863557 **Image available**
WPI Acc No: 2004-021388/200402
Related WPI Acc No: 2003-655845
XRAM Acc No: C04-006814
XRPX Acc No: N04-016428

Metal interconnection system disposed within via **comprises** first liner layer **of ion metal plasma-deposited titanium and** second **liner** layer **of ion metal plasma-deposited titanium nitride**

Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: LI W; TRIPATHI P P; WANG Z

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030203622	A1	20031030	US 2000617550	A	20000717	200402 B
			US 2003400252	A	20030327	

Priority Applications (No Type Date): US 2000617550 A 20000717; US 2003400252 A 20030327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030203622	A1		6	H01L-021/4763	Div ex application US 2000617550 Div ex patent US 6569751

Abstract (Basic): US 20030203622 A1

NOVELTY - A metal interconnection system disposed within a via (11) comprises a **first** liner **layer** (12) of ion metal plasma-deposited titanium; a **second** liner **layer** (14) of ion metal plasma-deposited titanium nitride; a third liner **layer** (16) of chemical vapor deposition titanium nitride; and a plug (18) of **tungsten** .

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of forming a metal interconnection system within a via by sequentially depositing a **first** liner **layer** of titanium using ion metal plasma deposition in an ion metal plasma deposition chamber; depositing a **second** liner **layer** of titanium nitride TixNy using ion metal plasma deposition in the chamber; depositing a third liner of titanium nitride using chemical vapor deposition in a **second** deposition chamber; and depositing a plug of **tungsten** .

USE - As metal interconnection system disposed within a via.

ADVANTAGE - The system reduces the contact resistance in a via by reducing the oxides that form on the titanium liner **layer** . Because the **second** liner **layer** of TixNy is deposited in the same chamber as the **first** liner **layer** of titanium, there is no opportunity for the **first** liner **layer** of titanium to oxidize to titanium oxide. Because the TixNy is deposited using ion metal plasma deposition, there is no cusping at the top of the via structure.

DESCRIPTION OF DRAWING(S) - The figure shows a partial cross-**sectional** view of a via filled with a metallization interconnection system.

Via (11)
First liner **layer** (12)
Second liner **layer** (14)
Third liner **layer** (16)
Plug (18)
Sidewalls (20)
Lower conduction **layer** (22)

pp; 6 DwgNo 1/1
Technology Focus:
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Dimensions: The **first** liner **layer** of ion metal plasma-deposited titanium has a thickness of 5-1000 Angstrom. The **second** liner **layer** of ion metal plasma-deposited TixNy has a thickness of 1-3000 Angstrom. Preferred Method: Depositing a **first** liner **layer** of titanium comprises placing a substrate containing the via within an ion metal plasma deposition chamber that contains a titanium target; evacuating the ion metal plasma deposition chamber to a **first** base pressure; introducing a **first** flow of argon to the ion metal plasma deposition chamber at 0.5-200 standard cubic centimeters per minute (sccm) and 10-4 - 0.1 Torr; biasing the substrate to 0 - -400 V; and energizing a plasma within the ion metal plasma deposition chamber at 1-50 kW for 1-100 **seconds** . Depositing a **second** liner **layer** of TixNy comprises introducing 1-200 sccm nitrogen and 0.5-100 sccm argon at 10-4 - 0.1 Torr; biasing the substrate to 0 - -400 V; energizing the plasma within the ion metal plasma deposition chamber at 1-50 kW for 0.1-100 **seconds** ; and removing the substrate from the ion metal plasma deposition chamber.
Title Terms: METAL; INTERCONNECT; SYSTEM; DISPOSABLE; COMPRISE; **FIRST** ; LINING; **LAYER** ; ION; METAL; PLASMA; DEPOSIT; TITANIUM; **SECOND** ; LINING; **LAYER** ; ION; METAL; PLASMA; DEPOSIT; TITANIUM; NITRIDE
Derwent Class: L03; U11; V05
International Patent Class (Main): H01L-021/4763
International Patent Class (Additional): H01L-021/44
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C13
Manual Codes (EPI/S-X): U11-C05D3; U11-C05G2C; U11-D03B2; V05-F05C

27/9/8 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015863082 **Image available**
WPI Acc No: 2004-020913/200402
XRAM Acc No: C04-006551
XRPX Acc No: N04-016030
Integrated circuit in horizontal surface of semiconductor body comprises dielectric layer **, vertical hole, barrier** layer **and copper-doped** transition layer
Patent Assignee: TEXAS INSTR INC (TEXI); BRENNAN K D (BREN-I); JIANG Q (JIAN-I); TSU R (TSUR-I)
Inventor: BRENNAN K D; JIANG Q; TSU R
Number of Countries: 033 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030186543	A1	20031002	US 2002107630	A	20020327	200402	B
EP 1351291	A2	20031008	EP 2003100707	A	20030319	200402	
JP 2004006748	A	20040108	JP 200384484	A	20030326	200405	
US 6693356	B2	20040217	US 2002107630	A	20020327	200413	

Priority Applications (No Type Date): US 2002107630 A 20020327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030186543	A1		11	H01L-021/4763	
EP 1351291	A2	E		H01L-021/768	

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

JP 2004006748 A 10 H01L-021/3205
US 6693356 B2 H01L-023/52

Abstract (Basic): US 20030186543 A1

NOVELTY - An integrated circuit has:

(a) dielectric **layer** over semiconductor body;

(b) vertical hole through dielectric **layer** and having sidewalls and **bottom** ;

(c) barrier **layer** over dielectric **layer** including sidewalls and **bottom** and is operable to seal copper; and

(d) copper-doped **transition layer** over barrier **layer** and having resistivity higher than pure copper and operable to strongly bond to copper and barrier **layer** , the remainder of the hole being filled with copper.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(1) a method for fabricating integrated circuit in horizontal surface of semiconductor body comprising forming the dielectric **layer** (210-212), etching a vertical hole through the dielectric **layer** , depositing the barrier **layer** (201) over the dielectric **layer** , depositing the copper-doped **transition layer** over the barrier **layer** and filling the remainder of the hole with copper; and

(2) a method for completing the integrated circuit in the horizontal surface of the semiconductor body comprising forming interlevel dielectric **layer** over the body, forming intrametal dielectric **layer** over the interlevel dielectric **layer** , etching a vertical trench (202, 203) into the intrametal dielectric **layer** and a vertical via (204) into the interlevel dielectric **layer** , depositing barrier **layer** over the intrametal dielectric **layer** , depositing copper-doped **transition layer** over the barrier **layer** , removing the barrier **layer** and the **transition layer** from **bottom** of the via to expose metal line, and filling the remainder of the trench and via with copper.

USE - Used as Integrated circuit in horizontal surface of semiconductor body.

ADVANTAGE - Provides low cost method of fabricating copper metallizations and copper-filled via interconnections in single and dual damascene technology and improved degree of component reliability. The fabrication method is simple yet flexible for different semiconductor product families and wide spectrum of design and process variations. This is accomplished without extending production cycle time and using installed equipment so that no new investment in the new manufacturing machines is needed.

DESCRIPTION OF DRAWING(S) - The figure shows a cross- **section** through copper-filled trenches and **via lined** with barrier **layers** .

Barrier **layer** (201)

Trenches (202, 203)

Via (204)

Dielectric **layers** (210-212)

Further dielectric **layer** (220)

pp; 11 DwgNo 2A/7

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The hole comprises a trench and a via. The barrier **layer** seals the dielectric **layer** so that microvoids within the porous dielectric **layer** are prevented from coalescing into larger voids and copper is prevented from migrating from the hole into the dielectric **layer** . The **transition layer** provides electrical resistivity and current density to suppress electromitigation.

METALLURGY - Preferred Materials: The dielectric **layer** is made of a porous material of low dielectric constant. The barrier **layer** is

made of refractory metal consisting of titanium, tantalum, **tungsten** , molybdenum, chromium or their compounds. It is made of an insulating dielectric compound consisting of silicon carbon nitride, silicon carbide, titanium nitride, tantalum nitride, **tungsten** nitride, **tungsten** carbide, silicon nitride, titanium silicon nitride or tantalum silicon nitride. The **transition layer** consists of copper tantalum, copper chromium, copper magnesium, copper aluminum, copper silicon, copper beryllium, copper zirconium, copper nickel, copper zinc, copper silver, copper titanium or copper palladium.

Title Terms: INTEGRATE; CIRCUIT; HORIZONTAL; SURFACE; SEMICONDUCTOR; BODY; COMPRISE; DIELECTRIC; **LAYER** ; VERTICAL; HOLE; BARRIER; **LAYER** ; COPPER; DOPE; TRANSITION; **LAYER**

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/3205; H01L-021/4763; H01L-021/768; H01L-023/52

International Patent Class (Additional): H01L-021/44; H01L-023/48; H01L-023/532; H01L-029/40

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C10D; L04-C12C; L04-C13A; L04-C13B

Manual Codes (EPI/S-X): U11-C05D3

27/9/21 (Item 16 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015087140 **Image available**

WPI Acc No: 2003-147658/200314

Related WPI Acc No: 2002-673037

XRAM Acc No: C03-038070

XRPX Acc No: N03-116610

Bonding pad has partially completed silicon integrated circuit, first hollow square trench, barrier layer , **metal** layer , **cap** layer , second **dielectric** layer , **broken** line **hollow square** via **hole, and aluminum bonding pad**

Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)

Inventor: CHU T Y; HSIA C C; TSUI B; YANG T

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020149115	A1	20021017	US 2000713801	A	20001116	200314	B
			US 2002170124	A	20020612		
US 6566752	B2	20030520	US 2000713801	A	20001116	200336	
			US 2002170124	A	20020612		

Priority Applications (No Type Date): US 2000713801 A 20001116; US 2002170124 A 20020612

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020149115	A1		7	H01L-023/48	Div ex application US 2000713801 Div ex patent US 6426555
US 6566752	B2			H01L-029/40	Div ex application US 2000713801 Div ex patent US 6426555

Abstract (Basic): US 20020149115 A1

NOVELTY - A bonding pad comprises:

(i) a partially completed silicon integrated circuit;

(ii) a **first** trench in the shape of a hollow square;

(iii) a barrier **layer** ;

(iv) a metal **layer** ;

(v) a cap **layer** ;

(vi) a **second** dielectric **layer** ;

(vii) a via hole in the shape of a broken line hollow square that is disposed to lie entirely within the **first** hollow square; and

(viii) an aluminum bonding pad that fills and fully overlaps the via hole

DETAILED DESCRIPTION - A bonding pad comprises a partially completed silicon integrated circuit that includes an uppermost **layer** of a **first** dielectric material having a **first upper** surface; a **first** trench, having a **first** width, in the shape of a hollow square (54) that extends downwards from the **first** surface to a depth; a barrier **layer** (41) over the **upper** surface and including the **first** trench; a metal **layer** that fills the **first** trench; a cap **layer** (42) over the **upper** surface and the metal **layer** ; a **second** dielectric **layer** over the cap **layer** and having a **second upper** surface; a via hole (32), having a **second** width less than the **first** width, in the shape of a broken line hollow square that is disposed to lie entirely within the **first** hollow square and that extends below the **second upper** surface, through the **second** dielectric **layer** and the cap **layer** , to the metal **layer** ; and an aluminum bonding pad on the **second upper** surface that fills and fully overlaps the via hole.

An INDEPENDENT CLAIM is included for a process of manufacturing the bonding pad, comprising providing the partially completed silicon integrated circuit having as its uppermost **layer** a **first** dielectric **layer** (15) having a **first upper** surface; forming the **first** trench in the shape of the hollow square that extends downwards from the **first upper** surface to the depth; depositing the barrier **layer** over the **upper** surface and the trench; overfilling the trench with metal and then planarizing, thus forming a damascene structure where the trench is just filled with metal; depositing a cap **layer** over the **upper** surface, including all exposed metal, followed by the **second** dielectric **layer** ; forming the via hole in the shape of the broken line hollow square that is disposed to lie entirely within the **first** hollow square and that extends downwards from the **second upper** surface, through the **second** dielectric **layer** and the cap **layer** , to expose the metal **layer** ; and depositing an aluminum **layer** (33) on the **second upper**0 surface and then patterning and etching the aluminum to form the bonding pad. The pad fills and fully overlaps the via hole.

USE - As a bonding pad.

ADVANTAGE - The inventive bonding pad has a low parasitic capacitance, and transmits little or no stress to the underlying metal **layer** during bonding. It protects a damascene conductor from damage during electrical probing and wire bonding.

DESCRIPTION OF DRAWING(S) - The figure is a cross- **sectional** view of a bonding pad.

First dielectric **layer** (15)
Via hole (32)
Aluminum **layer** (33)
Barrier **layer** (41)
Cap **layer** (42)
Silicon oxide **layer** (43)
Silicon nitride **layer** (44)
Hollow square (54)
pp; 7 DwgNo 5/12

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The **second** dielectric **layer** comprises a silicon oxide **layer** (43) covered by a

silicon nitride **layer** (44). The barrier **layer** is tantalum nitride, tantalum, titanium nitride, or **tungsten** nitride. It is deposited to a thickness of 300-1000Angstrom. The cap **layer** is silicon nitride, and is deposited to a thickness of 300-1000Angstrom. The **first** dielectric **layer** is an inter-metal dielectric (IMD) from undoped silicate glass, fluorinated silicon glass, or low k materials.

Preferred Properties: The **first** trench has a width of 1-10 mum, and a depth of 0.5-2 mum. The via hole has a width of 0.5-9 mum. The separation distance between the square via holes is 0.5-1 mum. The silicon oxide and silicon nitride **layers** have a thickness of 0.5-1 mum, respectively.

METALLURGY - Preferred Component: The metal is copper, a copper manganese alloy or a copper aluminum alloy

Title Terms: BOND; PAD; COMPLETE; SILICON; INTEGRATE; CIRCUIT; **FIRST** ; HOLLOW; SQUARE; TRENCH; BARRIER; **LAYER** ; METAL; **LAYER** ; CAP; **LAYER** ; **SECOND** ; DIELECTRIC; **LAYER** ; BREAK; LINE; HOLLOW; SQUARE; HOLE; ALUMINIUM; BOND; PAD

Derwent Class: L03; U11; U13

International Patent Class (Main): H01L-023/48; H01L-029/40

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C10C; L04-C10D; L04-C13B

Manual Codes (EPI/S-X): U11-D03A; U13-E03

27/9/29 (Item 24 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014667375 **Image available**

WPI Acc No: 2002-488079/200252

XRAM Acc No: C02-138586

XRPX Acc No: N02-385698

Formation of robust dual damascene interconnects for use in integrated circuit device fabrication involves filling conductive line **and** via **trenches in separate copper depositions**

Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD (CHAR-N); CHARTERED SEMICONDUCTOR MFG INC (CHAR-N)

Inventor: CHA C L; GOH W L; GUPTA S; LIM Y K; SEE A; TSE M S

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6380084	B1	20020430	US 2000678621	A	20001002	200252	B
TW 502388	A	20020911	TW 2001119858	A	20010814	200336	

Priority Applications (No Type Date): US 2000678621 A 20001002

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6380084	B1		21	H01L-021/44	
TW 502388	A			H01L-021/768	

Abstract (Basic): US 6380084 B1

NOVELTY - Formation of robust dual damascene interconnects involves filling conductive **line** and **via** trenches in separate copper depositions.

DETAILED DESCRIPTION - Formation of robust dual damascene interconnects by de-coupling **via** and connective **line** trench filling involves:

(a) providing a conductive **layer** (42) overlying a semiconductor substrate (40);

(b) depositing a silicon nitride **layer** (50) overlying the

conductive **layer** ;
(c) depositing a **first** dielectric **layer** (52) overlying the silicon nitride **layer** ;
(d) depositing a shielding **layer** (56) overlying the **first** dielectric **layer** ;
(e) patterning the shielding **layer** , the **first** dielectric **layer** and the silicon nitride **layer** to form via trenches that expose a part of the conductive **layer** ;
(f) depositing a **first** barrier **layer** (60) overlying the conductive **layer** and lining the via trenches;
(g) filling the via trenches with a **first** copper **layer** ;
(h) polishing down the **first** copper **layer** and the **first** barrier **layer** to complete vias;
(i) depositing a **second** barrier **layer** (68) overlying the vias and the **first** dielectric **layer** ;
(j) patterning the **second** barrier **layer** and the shielding **layer** to form via caps overlying the vias;
(k) depositing a **second** dielectric **layer** (72) overlying the via caps and the **first** dielectric **layer** ;
(l) depositing a capping **layer** overlying the **second** dielectric **layer** ;
(m) patterning the capping **layer** and the **second** dielectric **layer** to form connective line trenches that expose a part of the via caps;
(n) depositing a third barrier **layer** (80) overlying the capping and the via caps and lining the connective line trenches;
(o) anisotropically etching down the third barrier **layer** and the via caps to form barrier sidewall spacers lining the connective line trenches and to expose a part of the **first** copper **layer** ;
(p) filling the connective line trenches with a **second** copper **layer** (84); and
(q) polishing down the **second** copper **layer** to complete connective lines for the dual damascene interconnects in the manufacture of the integrated circuit device.
USE - For forming robust dual damascene interconnects used in the fabrication integrated circuit devices.
ADVANTAGE - The invention provides a very manufacturable method for fabricating dual damascene structures in the manufacture of integrated circuit devices. Parasitic capacitance can be reduced through the elimination of silicon nitride etch stops. Copper vias and connective lines are filled separately to improve fill characteristics and performance. The copper via can be used as a seed **layer** for the deposition of the connective lines by plating.
DESCRIPTION OF DRAWING(S) - The figure shows schematically illustrates in cross- **sectional** representation of a robust dual damascene interconnect.
Substrate (40)
Conductive **layer** (42)
Silicon nitride **layer** (50)
First dielectric **layer** (52)
Shielding **layer** (56)
First barrier **layer** (60)
Second barrier **layer** (68)
Second dielectric **layer** (72)
Third barrier **layer** (80)
Second copper **layer** (84)
pp; 21 DwgNo 14/23
Technology Focus:
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The

barrier **layers** , shielding **layer** , and capping **layer** are each made of tantalum nitride, titanium nitride, titanium, titanium- **tungsten** -nitride, or composite of tantalum nitride consisting of both crystalline and amorphous tantalum nitride.

ELECTRONICS - Preferred Method: The filling of via trenches with a **first** copper **layer** (64) involves depositing a seed **layer** via physical vapor deposition (PVD) or chemical vapor deposition (CVD), preferably CVD, and then plating the **first** copper **layer** by electrochemical plating and electroless plating. The filling of via trenches with a **second** copper **layer** involves using the exposed part of the **first** copper **layer** as a seed **layer** and the **second** copper **layer** is plated using electrochemical plating or electroless plating. The step of filling the **second** copper **layer** to the connective line trenches involves depositing a palladium acetate seed **layer** and plating the **second** copper **layer** through electrochemical plating or electroless plating. The connective line trenches are deposited with the **second** copper **layer** using CVD.

Title Terms: FORMATION; ROBUST; DUAL; INTERCONNECT; INTEGRATE; CIRCUIT; DEVICE; FABRICATE; FILL; CONDUCTING; LINE; TRENCH; SEPARATE; COPPER; DEPOSIT
Derwent Class: L03; U11; U13
International Patent Class (Main): H01L-021/44; H01L-021/768
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C06; L04-C07B; L04-C07E; L04-C10; L04-C10D; L04-C12; L04-C12B; L04-C13B
Manual Codes (EPI/S-X): U11-C05C; U13-D

27/9/31 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014581167 **Image available**
WPI Acc No: 2002-401871/200243
XRAM Acc No: C02-113127
XRPX Acc No: N02-315022
Formation of metal interconnect levels **in integrated circuit by patterning** first **dielectric** layer **to form trenches for planned damascene interconnects, and depositing conductive barrier** layer **over** first **dielectric** layer **and lining trenches**
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: CHOOI S; GUPTA S; HONG S; ZHOU M S; ZHOU M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6352917	B1	20020305	US 2000598691	A	20000621	200243	B
SG 90775	A1	20020820	SG 20013336	A	20010605	200277	

Priority Applications (No Type Date): US 2000598691 A 20000621
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6352917	B1		44	H01L-021/4763	
SG 90775	A1			H01L-021/4763	

Abstract (Basic): US 6352917 B1
NOVELTY - Metal interconnect **levels** are formed by patterning a **first** dielectric **layer** to form trenches for planned damascene interconnects, depositing conductive barrier **layer** overlying the **first** dielectric **layer** and lining the trenches, and polishing down a metal **layer** and the barrier **layer** to confine them to the trenches

and the damascene interconnects.

DETAILED DESCRIPTION - Formation of metal interconnect **levels** involves depositing a **first** dielectric **layer** (132) overlying a semiconductor substrate, and comprising stack of dielectric materials. The **first** dielectric **layer** is patterned to form trenches for planned damascene interconnects. An insulating **layer** is deposited overlying the **first** dielectric **layer** and lining the trenches. The insulating **layer** is anisotropically etched down the insulating **layer** to form insulating **layer** spacers (409) on the sidewalls of the trenches. The presence of the insulating **layer** spacers prevents metal diffusion into the **first** dielectric **layer** . A conductive barrier **layer** (140) is deposited overlying the **first** dielectric **layer** and lining the trenches. A metal **layer** (144) is deposited overlying the conductive barrier **layer** and filling the trenches. The metal **layer** and the conductive barrier **layer** are polished down to confine the metal **layer** and the conductive barrier **layer** to the trenches and to the damascene interconnects. The damascene interconnects are patterned to form via plugs in an **upper portion** of the damascene interconnects by partially etching down the damascene interconnects, where a via mask overlies and protects **portions** of the damascene interconnects from the etching down, where a trench mask overlies and protects the **first** dielectric **layer** from metal contamination during the etching down, and where **portions** of the damascene interconnects partially etched down form conductive lines. A nonconductive barrier **layer** (164) is deposited overlying the **first** dielectric **layer** , the conductive **lines** , and the **via** plugs. A **second** dielectric **layer** (168, 172) is deposited overlying the nonconductive barrier **layer** and filling gaps caused by the patterning of the copper **layer** to complete the metal interconnect **level** in the manufacture of the integrated circuit device.

USE - For forming metal interconnect **levels** in the manufacture of an integrated circuit device.

ADVANTAGE - The invention provides an effective and very manufacturable method to form metal interconnect **levels** . It simplifies the barrier **layer** deposition process and the copper deposition process. It does not require the additional etch stop **layer** , thus reducing capacitive coupling. Since the via plugs are formed in the same metal **layer** as the underlying conductive lines, there is no misalignment.

DESCRIPTION OF DRAWING(S) - The figure shows schematically in cross **section** a metal interconnect.

Etch stopping **layer** (124)

First dielectric **layer** (132)

Conductive barrier **layer** (140)

Metal **layer** (144)

Nonconductive barrier **layer** (164)

Second dielectric **layer** (168, 172)

Insulating **layer** spacers (409)

pp; 44 DwgNo 21/42

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: Etching down of damascene interconnects comprises wet etching or plasma-assisted dry etching. An etch stopping **layer** (124) is deposited overlying the substrate before the **first** dielectric **layer** is deposited. A passivation **layer** is deposited overlying the damascene interconnects, the conductive barrier **layer** , and the **first** dielectric **layer** after the step of polishing down the metal **layer** and the barrier **layer** . The presence of the passivation **layer** prevents metal diffusion into the **first** dielectric **layer** .

INORGANIC CHEMISTRY - Preferred Materials: The metal **layer** comprises copper. The dielectric **layer** comprises undoped silicon dioxide, fluorine-doped silicon dioxide, phosphorus-doped silicon dioxide, boron-doped silicon dioxide, phosphorus and boron-doped silicon dioxide, carbon-doped silicon dioxide, hydrogen-doped silicon dioxide, or their porous combinations. The conductive barrier **layer** comprises titanium, titanium nitride, tantalum, tantalum nitride, **tungsten** nitride, ternary metal-silicon-nitride (WSixNy), and/or ternary metal-boron-nitride (WBxNy). The metal **layer** comprises copper, copper alloys, aluminum, or aluminum alloys. The insulating **layer** comprises silicon nitride, silicon oxynitride, silicon carbide, or boron nitride. The passivation **layer** comprises silicon nitride, silicon carbide, or silicon oxynitride.

ORGANIC CHEMISTRY - Preferred Materials: The dielectric **layer** comprises organic polymers.

Title Terms: FORMATION; METAL; INTERCONNECT; **LEVEL** ; INTEGRATE; CIRCUIT; PATTERN; **FIRST** ; DIELECTRIC; **LAYER** ; FORM; TRENCH; PLAN; INTERCONNECT; DEPOSIT; CONDUCTING; BARRIER; **LAYER** ; **FIRST** ; DIELECTRIC; **LAYER** ; LINING; TRENCH

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/4763

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C07; L04-C07E; L04-C10; L04-C12; L04-C13B; L04-C27

Manual Codes (EPI/S-X): U11-C07

27/9/47 (Item 42 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013796412 **Image available**

WPI Acc No: 2001-280623/200129

XRAM Acc No: C01-085089

XRPX Acc No: N01-200037

Formation of conductive wiring line **and** via **, by forming insulative** layer **, etching stop** layer **, insulative** layer **, opening, and trench, defining wiring line, removing mask and metal, and depositing and planarizing metal**

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)

Inventor: HUANG C; LAI Y; TSAI Y; WU H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6204096	B1	20010320	US 99272429	A	19990319	200129	B

Priority Applications (No Type Date): US 99272429 A 19990319

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6204096	B1		9	H01L-021/82	

Abstract (Basic): US 6204096 B1

NOVELTY - Conductive wiring **line** and **via** are formed by forming a **first** insulative **layer** , an etching stop **layer** , a **second** insulative **layer** , an opening, and a trench; depositing a **first** conductive metal; forming a photoresist mask; defining wiring line; removing the photoresist mask and the **first** conductive metal; depositing a **second** conductive metal; and planarizing the **second** conductive metal surface.

DETAILED DESCRIPTION - Formation of a conductive wiring **line** and

a **via** on a substrate (111) for a semiconductor device, includes (a) forming a **first** insulative **layer** (112) on the substrate; (b) forming an etching stop **layer** (113) on the **first** insulative **layer** ; (c) forming a **second** insulative **layer** (114) on the etching stop **layer** ; (d) forming an opening in the **second** insulative **layer** at a location where the via is desired, in which the opening penetrates through the **second** insulative **layer** into the etching stop **layer** ; (e) forming a trench in the **second** insulative **layer** at a location where the wiring is desired while simultaneously extending the opening through the etching stop **layer** and trough the **first** insulative **layer** , in which the trench is wider than and the entirely inclusive area of the opening; (f) depositing a **first** conductive metal in the opening and in the trench so that the **first** conductive metal totally fills the opening and the trench; (g) forming a photoresist mask on the **first** conductive metal; (h) defining wiring line on the surface of the **first** conductive metal as pattern **layer** ; (i) removing the photoresist mask and then the **first** conductive metal; (j) depositing simultaneously a **second** conductive metal (23) in the opening and in the trench so that the **second** conductive metal totally fills the opening and the trench; and (k) planarizing the surface of the **second** conductive metal. An INDEPENDENT CLAIM is also included for a method of controlling critical dimension of an integrated circuit device having multiple **level** conductive structures, including forming an interlayer dielectric on the substrate, forming an etching stop **layer** , forming a dielectric **layer** on the etching stop **layer** , patterning the dielectric **layer** to define as wiring line, depositing a **first** conductive metal **layer** , patterning the **first** conductive metal **layer** on the etching stop **layer** and then over the interlayer dielectric **layer** to define as wiring line, removing excess parts of the conductive metal, depositing a **second** conductive metal **layer** , and planarizing the surface of the integrated circuit device.

USE - The invention is used for forming a conductive wiring **line** and a **via** on a substrate for a semiconductor device.

ADVANTAGE - The invention allows easier formation of quite deep focus, provides thin critical dimension, and improves production reliability.

DESCRIPTION OF DRAWING(S) - The figure shows a structure formed by the method.

Substrate (111)

First insulative **layer** (112)

Etching stop **layer** (113)

Second insulative **layer** (114)

Conductive metal (23)

pp; 9 DwgNo 2H/2

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The insulative **layers** are oxide (preferably silicon oxide). The etching stop **layer** is silicon (oxy)nitride, or polysilicon. The conductive material comprises a metal chosen from aluminum, **tungsten** , and copper (or their alloy). Preferred Method: The opening and the trench are formed by an etching process (preferably a reactive ion etching process). The **first** conductive material is removed using a rate of one-tenth buffered hydrofluoric acid solution, or diluted potassium hydroxide solution.

Title Terms: FORMATION; CONDUCTING; WIRE; LINE; FORMING; INSULATE; **LAYER** ; ETCH; STOP; **LAYER** ; INSULATE; **LAYER** ; OPEN; TRENCH; DEFINE; WIRE; LINE; REMOVE; MASK; METAL; DEPOSIT; METAL

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/82

File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C06B; L04-C10A; L04-C13B
Manual Codes (EPI/S-X): U11-C05B9A; U11-C05D3; U11-C05G2C; U11-C07D2

27/9/56 (Item 51 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013052591 **Image available**
WPI Acc No: 2000-224446/200019
XRAM Acc No: C00-068581
XRPX Acc No: N00-168174
Forming structure on substrate by depositing two dielectric layers **one over the other on substrate, and etch mask having a via pattern on the top dielectric** layer **, for forming interconnect** lines **and** via **plugs using dual damascene techniques**
Patent Assignee: APPLIED MATERIALS INC (MATE-N)
Inventor: BROYDO S; HEY H P W; NAIK M B; PARIKH S A
Number of Countries: 024 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200010202	A1	20000224	WO 99US18034	A	19990809	200019	B
EP 1110241	A1	20010627	EP 99939712	A	19990809	200137	
			WO 99US18034	A	19990809		
TW 437040	A	20010528	TW 99113498	A	19990806	200172	
KR 2001072404	A	20010731	KR 2001701776	A	20010210	200209	
JP 2002522923	W	20020723	WO 99US18034	A	19990809	200263	
			JP 2000565566	A	19990809		
US 6514671	B1	20030204	US 98133075	A	19980812	200313	
			US 2000675989	A	20000929		

Priority Applications (No Type Date): US 98133075 A 19980812; US 2000675989 A 20000929
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200010202	A1	E	37	H01L-021/768	
Designated States (National): JP KR SG					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1110241	A1	E		H01L-021/768	Based on patent WO 200010202
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
TW 437040	A			H01L-023/522	
KR 2001072404	A			H01L-021/768	
JP 2002522923	W		40	H01L-021/768	Based on patent WO 200010202
US 6514671	B1			G03C-005/00	Div ex application US 98133075

Abstract (Basic): WO 200010202 A1
NOVELTY - Structure is formed on a substrate (310) by depositing two dielectric **layers** (314,316) of different etching characteristics, one over the other on the substrate. An etch mask with a via pattern is deposited on the **second layer** . It is anisotropically etched through the dielectric **layers** to form a via hole in the **first layer** . The etch mask is removed, and a trench is etched in the **second** dielectric **layer** .
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (A) a device comprising a substrate (310), two dielectric **layers** of different etching characteristics, a **first** region in the **first** dielectric 1layer (314) defining a via hole extending through the

first **layer** , and a **second** region in the **second** dielectric **layer** (316) defining a trench on the underlying via hole, which extends through the **second** dielectric **layer** ; where the via hole and the trench are adapted to contain a dual damascene structure; and (B) an apparatus for controlling the formation of a fabricated structure on a substrate, which comprises at least one controller to interact with several fabrication stations, and a data structure which causes the controller to control the formation of the fabricated structure.

USE - The invention is used for forming IC structure on a substrate, for the fabrication of semiconductor device interconnect **lines** and **via** plugs using dual damascene techniques.

ADVANTAGE - The invented method results in additional improved damascene fabrication techniques because the via etch does not require etching of very deep vias, as compared with prior art dual damascene techniques. It avoids the use of a timed etch, resulting in improved etch depth control, and also avoids the use of an etch stop **layer** between the inter-metal **layer** and the intra-metal dielectric **layers** , thus facilitating fabrication and resulting in quality improvements and cost reductions. It optimizes the mechanical, thermal, and electrical properties of the structure.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-**sectional** side view of the invented structure.

Substrate (310)

First dielectric **layer** (314)

Second dielectric **layer** (316)

Via plug (332)

pp; 37 DwgNo 3E/8

Technology Focus:

TECHNOLOGY FOCUS - POLYMERS - Preferred Material: The etch mask comprises photo resist masks, hard masks, or their combinations. It may be a silicon-based photosensitive material including plasma polymerized methylsilane which is patterned by exposure to radiation so that exposure causes the plasma polymerized methylsilane to form a hard mask comprising plasma polymerized methylsilane oxide. The **second** dielectric **layer** comprises amorphous fluorinated carbon, organic spin-on materials, spin-on-glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers, and/or divinyl siloxane benzocyclobutane.

INORGANIC CHEMISTRY - Preferred Materials: The **first** dielectric **layer** comprises SiO2 and/or fluorinated SiO2. The conductive material comprises metals, alloys, metallic superconductors, or nonmetallic superconductors. It comprises copper, silver, aluminum, **tungsten** , their alloys, nickel/germanium or yttrium/barium/copper oxides.

Extension Abstract:

EXAMPLE - In an EMBODIMENT of the method, the **first** dielectric **layer** material has a dielectric constant of 3.5-8, and the **second** dielectric **layer** material has a dielectric constant of 1-3.5. The trench pattern is anisotropically etched through a **second** dielectric **layer** in an oxygen-based etch chemistry. The trench and the via hole are filled by chemical vapor deposition, physical vapor deposition, electroplating, or electroless plating. A cap **layer** is interposed between the substrate and the **first** dielectric **layer** .

Title Terms: FORMING; STRUCTURE; SUBSTRATE; DEPOSIT; TWO; DIELECTRIC; **LAYER** ; ONE; SUBSTRATE; ETCH; MASK; PATTERN; TOP; DIELECTRIC; **LAYER** ; FORMING; INTERCONNECT; LINE; PLUG; DUAL; TECHNIQUE

Derwent Class: A85; L03; P83; U11

International Patent Class (Main): G03C-005/00; H01L-021/768; H01L-023/522

International Patent Class (Additional): H01L-021/28; H01L-021/3065; H01L-023/485; H01L-039/06; H01L-039/24

File Segment: CPI; EPI; EngPI

Manual Codes (CPI/A-N): A12-E07C; A12-L02B2; L04-C06A; L04-C07; L04-C13A
Manual Codes (EPI/S-X): U11-C05D3; U11-C05G2C
Polymer Indexing (PS):
<01>
001 018; D50 D81 F86 F20 D11 D10 G2277-R G2266 D01 Si 4A; H0000; K9427; P1445-R F81 Si 4A; L9999 L2573 L2506
002 018; D18-R D69 F- 7A; P0964-R F34 D01; H0293
003 018; D34 D77 D57 D58 D93 F81 F86 D54 D51 D12 D10 D21 D18 G0964 G0817 D01 G2302 G2299 G2266 Si 4A; P0066; P0044; P1967 P0044 D01 D18 D21
004 018; ND01; Q9999 Q7863; Q9999 Q7476 Q7330; B9999 B3203-R B3190; B9999 B3214 B3203 B3190; Q9999 Q8684 Q8673 Q8606

27/9/60 (Item 55 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011492155 **Image available**
WPI Acc No: 1997-470061/199743
XRAM Acc No: C97-149327
XRPX Acc No: N97-392229
Forming a tungsten **@ plug in a semiconductor device - where over-etching loss of** tungsten **@ in vias is prevented while removing** tungsten **residues and mis-connection and reliability problems are avoided**
Patent Assignee: HYUNDAI ELECTRONICS IND CO LTD (HYUN-N)
Inventor: KIM D; LEE J; PAK S; KIM D S; LEE J I; PARK S H
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5668064	A	19970916	US 96606305	A	19960223	199743	B
TW 348276	A	19981221	TW 96102077	A	19960223	199921	
CN 1140332	A	19970115	CN 96105584	A	19960224	200044	
KR 187666	B1	19990601	KR 953610	A	19950224	200055	

Priority Applications (No Type Date): KR 953610 A 19950224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5668064	A		7	H01L-021/60	
TW 348276	A			H01L-021/302	
CN 1140332	A			H01L-021/74	
KR 187666	B1			H01L-021/768	

Abstract (Basic): US 5668064 A

A method of forming a **tungsten** plug connecting **upper** and **lower** metal **lines** in a **via** hole formed by etching an insulating film in a semiconductor device comprises forming a barrier metal **layer** (15) and then a **tungsten layer** on the insulating film (12) including the via. A photoresist pattern covering the via hole is formed on the **tungsten** , which is isotropically etched and then anisotropically etched so that the barrier **layer** is exposed. The photoresist is removed and **tungsten** projections above the plug removed to leave the plug within the via (16F).

Also claimed is a method as above in which the anisotropic etching is performed after the photoresist mask is removed.

USE - In forming **tungsten** plugs in vias connecting metal lines of sub-micron width

ADVANTAGE - **Tungsten** residues, which may bridge metal lines, are removed without overetching the plug, which avoids misconnections and loss of reliability.

Dwg.3D/4
Title Terms: FORMING; **TUNGSTEN** ; PLUG; SEMICONDUCTOR; DEVICE; ETCH; LOSS; **TUNGSTEN** ; VIAS; PREVENT; REMOVE; **TUNGSTEN** ; RESIDUE; MIS; CONNECT; RELIABILITY; PROBLEM; AVOID
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/302; H01L-021/60; H01L-021/74; H01L-021/768
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C13B
Manual Codes (EPI/S-X): U11-C05G2C
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